SERIES
681XXA
SYNTHESIZED SWEEP GENERATOR

MAINTENANCE MANUAL

WILTRON

490 JARVIS DRIVE
MORGAN HILL, CA 95037-2809

P/N: 10370-10252
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WARRANTY

The WILTRON product(s) listed on the title page is (are) warranted against defects in materials and workmanship for one year from the date of shipment, except for YIG-tuned oscillators and all WILTRON manufactured microwave components, which are warranted for two years.

WILTRON's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to WILTRON for warranty repairs. Obligation is limited to the original purchaser. WILTRON is not liable for consequential damages.

LIMITATION OF WARRANTY

The foregoing warranty does not apply to WILTRON connectors that have failed due to normal wear. Also, the warranty does not apply to defects resulting from improper or inadequate maintenance by the Buyer, unauthorized modification or misuse, or operation outside of the environmental specifications of the product. No other warranty is expressed or implied, and the remedies provided herein are the Buyer's sole and exclusive remedies.

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General Information

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Figure 1-1. *Series 681XXA Synthesized Sweep Generator*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides service information for all models of the Series 681XXA Synthesized Sweep Generator. The service information includes replaceable parts information, functional circuit descriptions, block diagrams, performance verification tests, and procedures for calibration, troubleshooting, and assembly/subassembly removal and replacement. (Throughout this manual, the terms *681XXA* and *sweep generator* are used interchangeably to refer to the instrument.) Manual organization is shown in the table of contents.

1-2 INTRODUCTION

This chapter provides a general description of the Series 681XXA Synthesized Sweep Generator, its identification number, related manuals, and options. Information is included concerning level of maintenance, replaceable subassemblies and RF components, exchange assembly program, and preventive maintenance. Static-sensitive component handling precautions and lists of exchangeable subassemblies and recommended test equipment are also provided.

1-3 DESCRIPTION

The Series 681XXA Synthesized Sweep Generators are microprocessor-based, synthesized signal sources with high resolution phase-lock capability. They generate both broad (full range) and narrow band sweeps and discrete CW frequencies across the frequency range of 10 MHz to 40 GHz. All functions of the sweep generator are fully controllable locally from the front panel or remotely (except for power on/standby) via the IEEE-488 General Purpose Interface Bus (GPIB).

The series presently consists of four models covering a variety of frequency ranges and power levels. Table 1-1 (page 1-4) lists models, frequency ranges, and maximum leveled output.

Table 1-1. *Series 681XXA Models*

681XXA Model	Frequency (GHz)	Output Power	Output Power w/Optional Attenuator
68137A	2.0-20.0 GHz	+13 dBm	+10 dBm
68137A w/Hi Pwr Option	2.0-20.0 GHz	+17 dBm	+14 dBm
68147A	0.01-20.0 GHz	+13 dBm	+10 dBm
68147A w/Hi Pwr Option	0.01-2.0 GHz 2.0 -20.0 GHz	+13 dBm +17 dBm	+10 dBm +14 dBm
68163A	2.0-40.0 GHz	+6 dBm	+2 dBm
68169A	0.01-40.0 GHz	+6 dBm	+2 dBm

1-4 IDENTIFICATION NUMBER

All WILTRON instruments are assigned a unique six-digit ID number, such as “301001”. The ID number is imprinted on a decal that is affixed to the rear panel of the unit. Special-order instrument configurations also have an additional *special* serial number tag attached to the rear panel of the unit.

When ordering parts or corresponding with AWSC Customer Service, please use the correct serial number with reference to the specific instrument’s model number (i.e., Model 68147A Synthesized Sweep Generator, Serial No. 301001).

1-5 RELATED MANUALS

This is one of a three manual set that consists of an Operation Manual (OM), a Programming Manual (PM), and a Maintenance Manual (MM). The OM provides instructions for front panel operation of the 681XXA. It also includes general information, performance specifications, installation instructions, and operation verification procedures. The WILTRON part number for the OM is 10370-10250.

The PM provides information for operating the series 681XXA sweep generator with commands sent from an external controller via the IEEE 488 General Purpose Interface Bus (GPIB). It contains a general description of the GPIB and bus data transfer and control functions, a comlete listing and description of the 681XXA command codes, and several examples of bus programming. The WILTRON part number for the PM is 10370-10254.

1-6 OPTIONS

The following instrument options are available.

- **Option 1, Rack Mounting**. Rack mount kit containing a set of track slides (90° tilt capability), mounting ears, and front panel handles for mounting the instrument in a standard 19-inch equipment rack.
- **Option 2A, 110 dB Step Attenuator**. Adds a 10 dB per step attenuator with a 110 dB range for models having a high-end frequency of ≤20 GHz. Output power is selected directly in dBm on the front panel (or via GPIB) over a 122 dB range. Rated output power is reduced by 3 dB.
- **Option 2B, 110 dB Step Attenuator**. Adds a 10 dB per step attenuator with a 110 dB range for models having a high-end frequency of ≤40 GHz. Output power is selected directly in dBm on the front panel (or via GPIB) over a 122 dB range. Rated output power is reduced by 4 dB.
- **Option 9K, Rear Panel RF Output**. Adds an RF output connector (K-Connector ®, female) to the rear panel and deletes the RF output connector on the front panel.
- **Option 11, 0.1 Hz Frequency Resolution**. Provides frequency resolution of 0.1 Hz.
- **Option 14, WILTRON 360B VNA Compatibility**. Modifies rack mounting hardware to mate unit in a Wiltron 360B VNA console.
- **Option 15, High Power Output**. Adds high-power RF components to the instrument providing 50 mW RF output power in the 2–20 GHz frequency range. This option is only available for models 68137A and 68147A .
- **Option 16, High-Stability Time Base**. Adds an ovenized, 10 MHz crystal oscillator with $<5 \times 10^{-10}$/day frequency stability.
- **Option 17, No Front Panel**. Deletes the front panel for use in remote control applications where a front panel display or keyboard control are not needed.

K Connector ® is a registered trademark of WILTRON Company.

1-7 STARTUP CONFIGURATIONS

The 681XXA comes from the factory with a jumper across pins 1 and 2 of Motherboard connector J3 (Figure 1-2). In this configuration, connecting the instrument to line power automatically places it in operate mode (front panel OPERATE LED on).

The startup configuration can be changed so that the 681XXA comes up in standby mode (front panel STANDBY LED on) when it is connected to line power. Change the startup configuration as follows:

Step 1 Disconnect the instrument from line power.

Step 2 Remove the top cover from the 681XXA. (Refer to Chapter 6 for instructions).

Step 3 Locate Motherboard connector J3 and remove the jumper from across pins 1 and 2. It is accessable through an opening in the RF deck that is located next to the directional coupler.

Step 4 Install the jumper across pins 3 and 4 of connector J3.

Step 5 Install the top cover and connect the 681XXA to line power. The instrument should come up in standby mode.

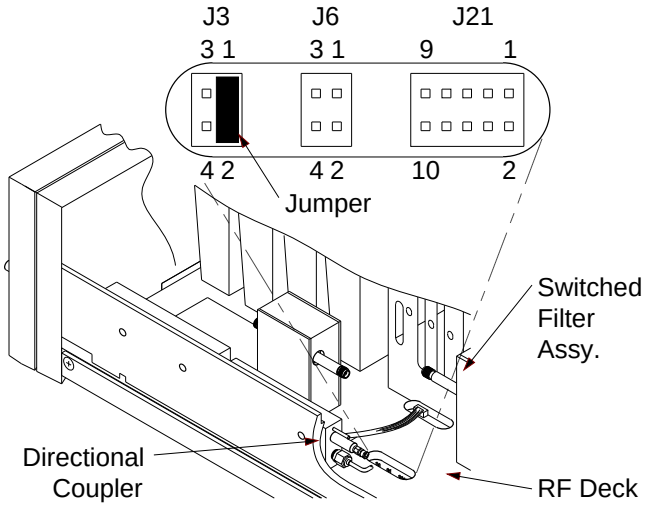


Figure 1-2. *Startup Configuration of Motherboard Connector J3*

1-8 LEVEL OF MAINTENANCE

Maintenance of the 681XXA consists of:

- Troubleshooting the sweep generator to a replaceable subassembly or RF component.
- Repair by replacing the failed subassembly or RF component.
- Calibration
- Preventive maintenance.

Troubleshooting The 681XXA firmware includes internal diagnostics that self-test most of the internal assemblies of the sweep generator. When the 681XXA fails self-test, one or more error messages are displayed to aid in troubleshooting the failure to a replaceable subassembly or RF component. Chapter 5–Troubleshooting lists and describes the self-test error messages and provides procedures for isolating 681XXA failures to a replaceable subassembly or RF component.

Repair Most sweep generator failures are field repairable by replacing the failed subassembly or RF component. Detailed instructions for removing and replacing failed subassemblies and RF components are provided in Chapter 6–Removal and Replacement Procedures.

Calibration The 681XXA may require calibration after repair. Refer to Chapter 4–Calibration for a listing of calibration requirements and calibration procedures.

Preventive Maintenance Preventive maintenance on the 681XXA consists of cleaning the fan honeycomb filter, described in paragraph 1-9.

1-9 PREVENTIVE MAINTENANCE

The sweep generator must always receive adequate ventilation. Check and clean the rear panel fan honeycomb filter periodically. Clean the fan honeycomb filter more frequently in dusty environments. Clean the filter as follows.

Step 1 Remove the four thumb nuts holding the fan grill in place (Figure 1-3).

Step 2 Remove the fan grill.

Step 3 Vacuum the honeycomb filter to clean it.

Step 4 Install the fan grill and four thumb nuts.

Step 5 Tighten the thumb nuts securely.

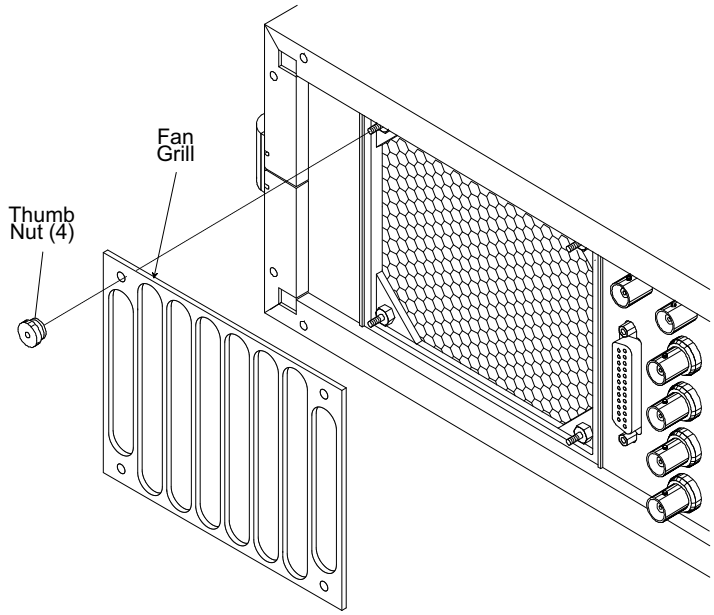


Figure 1-3. *Removing/Replacing the Fan Grill*

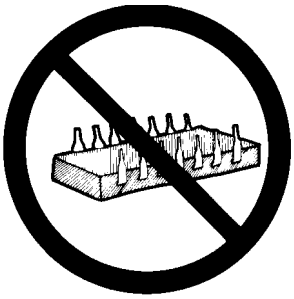
1-10 STATIC-SENSITIVE COMPONENT HANDLING PRECAUTIONS

The 681XXA contains components that can be damaged by static electricity. Figure 1-4 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

NOTE

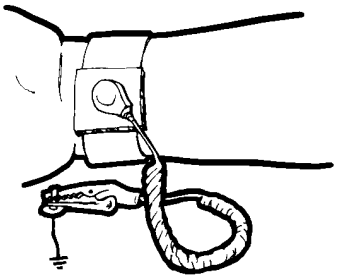
Use of a grounded wrist strap when removing and/or replacing subassemblies or components is strongly recommended.

1. Do not touch exposed contacts on any static sensitive component.



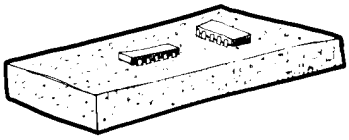
2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

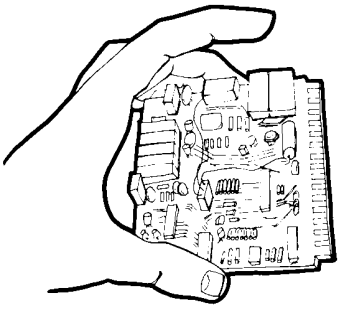


4. Wear a static-discharge wristband when working with static sensitive components.

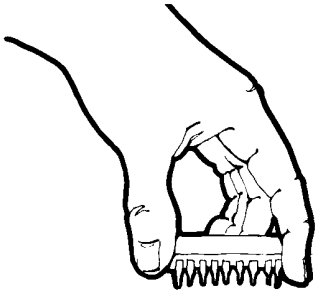
5. Label all static sensitive devices.



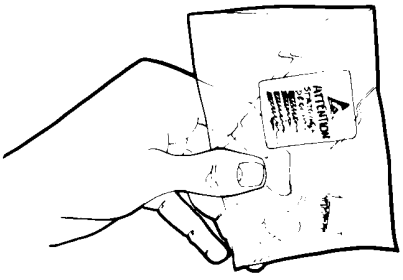
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:
    - Keep workspaces clean and free of any objects capable of holding or storing a static charge.
    - Connect soldering tools to an earth ground.
    - Use only special anti-static suction or wick-type desoldering tools.

Figure 1-4. Static-Sensitive Component Handling Precautions

1-11 RECOMMENDED TEST EQUIPMENT

Table 1-2 provides a list of recommended test equipment needed for the performance verification, calibration, and troubleshooting procedures presented in this manual.

Table 1-2. *Recommended Test Equipment (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USAGE (1)
Spectrum Analyzer, with Diplexer Assy and External Mixers	*Frequency Range:* 0.01 to 40 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794, with External Mixers: WM780K (18 to 26.5 GHz) WM780A (26.5 to 40 GHz) Diplexer Assy: 015-0385-00	C, P, T
Spectrum Analyzer	*Frequency Range:* 20 Hz to 40 MHz *Resolution Bandwidth:* ≤3 MHz	Hewlett-Packard, Model 3585B	C, P
Frequency Counter, with External Mixer	*Frequency Range:* 0.01 to 40 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz *Other:* External Time Base Input	EIP Microwave, Inc. Model 578A, with External Mixer: Option 91 (26.5 to 40 GHz)	C, P
Power Meter, with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	Hewlett-Packard Model 436A, with Power Sensor: HP 8487A (0.01 to 50 GHz)	P
Digital Multimeter	*Resolution:* 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% +2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% +100 counts (to 20 kHz) *AC Input Impedance:* 1 MΩ	John Fluke, Inc., Model 8840A, with Option 8840A-09 (True RMS AC)	C, T
Frequency Standard	*Frequency:* 10 MHz *Accuracy:* 1 x 10^{-10} parts/day	Spectracom Corp., Model 8161	P
Function Generator	*Output Voltage:* 1 volt peak-to-peak *Functions:* 0.5 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 8116A	C
Modulation Analyzer	*Frequency Input:* 10 MHz (or the IF of the Spectrum Analyzer) *AM Depth:* 0% to 90% *AM Modulation Rates:* DC to 100 kHz *Filters:* 50 Hz lowpass, 15 kHz highpass	Hewlett-Packard, Model 8902A	C
Oscilloscope	*Bandwidth:* DC to 150 MHz *Vertical Sensitivity:* 2mV/division *Horizontal Sensitivity:* 50 ns/division	Tektronix, Inc. Model 2445	P, T

Table 1-2. *Recommended Test Equipment (2 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USAGE (1)
Mixer	*Frequency Range:* 1 to 26 GHz	RHG Electronics Laboratory, Inc. Model DMS1-26A	P
Scalar Network Analyzer, with RF Detector	*Frequency Range:* 0.01 to 40 GHz	WILTRON, Model 562, with RF Detector: 560-7K50 (0.01 to 40 GHz)	C, T
Adapter	K (male) to 2.4 mm (female) Adapts the Power Sensor, HP 8487A, to the 681XXA RF OUTPUT connector	Hewlett-Packard Part Number: HP 11904D	P
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	WILTRON, Model 41KC-10	C, P
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	WILTRON, Model 41KC-20	P
RF Detector	*Frequency Range:* 0.01 to 40 GHz *Output Polarity:* Negative	WILTRON, Model 75KC50 (K input/BNC output connectors)	C, T
Personal Computer	*PC Configuration:* IBM AT or compatible *Operating System:* Windows 3.1 *Accessories:* Mouse	Any common source	C
Serial Interface Assy	Provides serial interface between the PC and the 681XXA.	WILTRON P/N: T1678	C
Tee	*Connectors:* 50Ω BNC	Any common source	C, P
Cables	*Connectors:* 50Ω BNC	Any common source	C, P, T

NOTES: (1) P = Performance Verification Tests (Chapter 3); C = Calibration (Chapter 4); T = Troubleshooting (Chapter 5)

1-12 EXCHANGE ASSEMBLY PROGRAM

WILTRON maintains an exchange assembly program for selected 681XXA subassemblies and RF components. If a malfunction occurs in one of these subassemblies, the defective unit can be exchanged. Upon receiving your request, WILTRON will ship the exchange subassembly or RF component to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF components are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call your local WILTRON service center. Refer to Table 1-5, on page 1-15, for a list of current WILTRON service centers.

1-13 REPLACEABLE SUBASSEMBLIES AND PARTS

Table 1-3 lists those replaceable subassemblies and RF components of the 681XXA that are presently covered by the WILTRON exchange assembly program. Table 1-4, on page 1-14, lists common replaceable parts for the 681XXA that are not presently on the exchange assembly program.

All parts listed in Tables 1-3 and 1-4 may be ordered from your local WILTRON service center.

Table 1-3. *Replaceable Subassemblies and RF Components*

SUBASSEMBLY OR PART NAME	WILTRON PART NUMBER
Printed Circuit Board Assemblies	
A1, A2 Front Panel Assy	D37337-51
A3 Reference Loop PCB Assy	D37403-3
A4 Coarse Loop PCB Assy	D37404-3
A5 Fine Loop PCB Assy	D37405-3
A5 Fine Loop PCB Assy (w/Option 11)	ND39665
A6 Square Wave Generator PCB Assy	D37406-3
A7 YIG Loop PCB Assy	D37407-3
A9 PIN Control PCB Assy	D37409-3
A9-1 PIN Control PCB Assy	D37432-3
A10 ALC PCB Assy	D37410-3
A11 AM/FM PCB Assy	D37411-3
A12 Analog Instruction PCB Assy	D37412-3
A13 YIG Driver PCB Assy	D37413-3
A14 FEU Driver PCB Assy	D37414-3
A14-1 SDM Driver PCB Assy	D37434-3
A15 Regulator PCB Assy	D37415-3
A16 CPU Interface PCB Assy	D37416-3
A17 CPU PCB Assy	A37417
A18 Power Supply PCB Assy	D37418-3
A19 Power Conditioner PCB Assy	D37431-3
A21 Line Filter/Rectifier PCB Assy	ND39664
A21-1 BNC/AUX I/O Connector PCB Assy	ND39672
10 MHz Crystal Oscillator Assy	D37332
RF Components	
YIG-Tuned Oscillator, 2 to 20 GHz	C21640
Down Converter	C37328-7
Down Converter	D24250
Frequency Extension Unit, 20 to 40 GHz	D21230
Switched Doubler Module, 20 to 40 GHz	D24870
Coupler	D21602
Switched Filter (Replaced by P/N D24211)	D25030
Switched Filter	D24211
Switched Filter	D26932
Switched Filter (w/Option 15)	D26340
Output Connector Assy	ND39077
Step Attenuator, 110 dB, 20 GHz	D25081
Step Attenuator, 110 dB, 40 GHz	D25080

Table 1-4. *Common Replaceable Subassemblies and Parts*

SUBASSEMBLY OR PART NAME	WILTRON PART NUMBER
Cap, Protective (for RF Output Connector)	A20304
Cover, Top	D37049
Cover, Bottom	D37050
Cover, CPU Housing	C37063
Cover, Main Card Cage	D37064
Cover, Power Supply Housing	C37062
EMI Gasket (for Side Rails and Front Panel Assy)	790-391
Fan, Assembly	A39817
Fan Grill	B39434
Thumb Nut (for Fan Grill)	790-193
Foot, Rear	D37051
Foot, Bottom	D37052
Tilt Bail, Bottom Foot	B37058
Fuse, 5A, 3AG Slow Blow	631-33
Gasket, RFI (“O”rings for MCX connectors)	790-393
Handle, Front	C37117
Trim Strip (for Front Handle)	B31661
Line Module Assembly	A39816
Shield, High Voltage Line Filter	B37061
Strap Handle	B37056
Insert (for Strap Handle)	B37057
End Cap (for Strap Handle)	B37105
Screws (for End Cap)	900-714

Table 1-5. *WILTRON Service Centers*

UNITED STATES
WILTRON COMPANY
490 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 778-2000
Telex: 285227 WILTRON MH
FAX: 408-778-0239

ANRITSU WILTRON SALES COMPANY
685 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
FAX: 408-776-1744

ANRITSU WILTRON SALES COMPANY
10 Kingsbridge Road
Fairfield, NJ 07004
Telephone: (201) 227-8999
FAX: 201-575-0092

AUSTRALIA
WILTRON PTY. LTD.
Level 2, 410 Church Street
North Parramatta
NSW 2151 Australia
Telephone: 026-30-81-66
Fax: 026-83-68-84

BRAZIL
ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440-Sa;a 2.401-Botafogo
2225-Rio de Janeiro-RJ-Brasil
Telephone: 021-28-69-141
Fax: 021-53-71-456

CANADA
ANRITSU WILTRON INSTRU-MENTS LTD.
215 Stafford Road, Unit 102
Nepean, Ontario K2H 9C1
Telephone: 613-828-4090
FAX: 613-828-5400

CHINA
WILTRON BEIJING SERVICE CENTER
416W Beijing Fortune Building
5 Dong San Huan Bei Lu
Chao Yang Qu, Beijing 100004, China
Telephone: 86-1-50-17-559
FAX: 86-1-50-17-558

FRANCE
ANRITSU WILTRON S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-44-66-546
FAX: 016-44-61-065

GERMANY
ANRITSU WILTRON GmbH
Rudolf Diesel Strabe 17
8031 Gilching
Telephone: 08-10-58-055
Telex: 841-528523
FAX: 08-10-51-700

INDIA
ACCUTROL SYSTEMS PRIVATE LIMITED
Nirmal, 15th Floor
Narimen Point
Bombay 400 021
Telephone: 011-91-22-202-2220
FAX: 011-91-22-202-9403

ISRAEL
TECH-CENT, LTD
Haarad St. No. 7, Ramat Haahayal
Tel-Aviv 69701
Telephone: 03-64-78-563
FAX: 03-64-78-334

ITALY
ANRITSU WILTRON Sp.A
Roma Office
Via E. Vittorini, 129
00144 Roma EUR
Telephone: 06-50-22-666
FAX: 06-50-22-4252

JAPAN
ANRITSU CORPORATION
1800 Onna Atsugi-shi
Kanagawa-Prf. 243 Japan
Telephone: 0462-23-1111
FAX: 0462-25-8379

KOREA
WILTRON CORPORATION
#2103 Korea World Trade Center
159-1 Samsung-Dong
Kangnam-ku, Seoul
Telephone: 02-551-2250
FAX: 02-551-4941

SWEDEN
WILTRON AB
Box 247
S-127 25 Skarholmen
Telephone: 08-74-05-840
Telex: 854-81-35-089
FAX: 08-71-09-960

TAIWAN
WILTRON CO., LTD.
8F, No. 96, Section 3
Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Telephone: 02-515-6050
FAX: 02-509-5519

UNITED KINGDOM
ANRITSU WILTRON LTD.
Capability Green
Luton, Bedfordshire
LU1 3LU, England
Telephone: 05-82-41-88-53
Telex: 851-826750
FAX: 05-82-31-303

Chapter 2
Functional Description

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Chapter 2
Functional Description

2-1 INTRODUCTION

This chapter provides functional descriptions of the major subsystems that are contained in each model of the sweep generator. In addition, the operation of the main circuits within each subsystem is described so that the reader may better understand the function of the subsystem as part of the overall operation of the 681XXA. Block diagrams are included to supplement the written descriptions.

2-2 681XXA MAJOR SUBSYSTEMS

The sweep generator circuitry consists of various distinct subsystems that are contained on one or more printed circuit board (PCB) assemblies or in microwave components located on the RF deck. The following paragraphs identify the subsystems that make up the sweep generator and provide a brief description of each. Figure 2-1 (page 2-6) is an overall block diagram of the 681XXA.

NOTE

There are two instrument configurations for models with a frequency range above 20 GHz. Models having serial numbers below 320001 contain the 20-40 GHz Frequency Extension Unit (FEU), the A9 PIN Control PCB, and the A14 Doubler Driver PCB. This configuration is shown in Sheet 2 of Figure 2-1. Models having serial numbers 320001 and above contain the 20-40 GHz Switched Doubler Module (SDM), the A9-1 PIN Control PCB, and the A14-1 SDM Driver PCB. Sheet 3 of Figure 2-1 shows this configuration.

Digital Control

This circuit subsystem consists of the A17 CPU and A16 CPU Interface PCBs. The central processor unit is the main controller for the sweep generator. This controller directly or indirectly controls all functions of the 681XXA. The CPU is directly linked via a dedicated data and address bus to the A9 or A9-1 PIN Control PCB, the A10 ALC PCB, the A11 AM/FM PCB, the A12 Analog Instruction PCB, and the A16 CPU Interface PCB. It has a GPIB interface that allows it to communicate with external devices over the GPIB and a serial interface to a serial terminal port on the rear panel.

The CPU is indirectly linked via the A16 CPU Interface PCB to the A2 Front Panel PCB, the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5 Fine Loop PCB, and the A6 Square Wave Generator

PCB. The A16 PCB contains circuitry to perform parallel-to-serial and serial-to-parallel data conversion. It also contains circuitry for many of the rear panel signals, a 13-bit resolution DVM, and decoder circuitry for the front panel rotary data knob optical encoder.

Front Panel

This circuit subsystem consists of the the A1 Front Panel PCB, the A2 Front Panel Control PCB, and the Liquid Crystal Display (LCD). This subsystem interfaces the front panel LCD, LEDs, keys, and rotary data knob to the CPU via the A16 CPU Interface PCB. The A1 Front Panel PCB contains the keyboard matrix of conductive rubber switches. The A2 Front Panel Control PCB has circuitry to control the LCD dot-matrix display, turn the front panel LEDs on and off, and convert keyboard switch matrix signals to serial keycode. It also contains the standby/operate line switch logic circuit and the optical encoder for the rotary data knob.

Frequency Synthesis

The frequency synthesis subsystem consists of the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5 Fine Loop PCB, the A7 YIG Loop PCB, and the A11 AM/FM PCB. It provides the reference frequencies and phase lock circuits for precise control of the YIG-tuned oscillator frequencies.

- The A3 Reference Loop PCB supplies the stable 10 MHz and 500 MHz reference frequency signals for the rest of the frequency synthesis system.
- The A4 Coarse Loop PCB generates coarse tuning frequencies of 439 to 490 MHz for use by the YIG Loop.
- The A5 Fine Loop PCB provides fine tuning frequencies of 22 to 40 MHz for use by the YIG Loop.
- The A7 YIG Loop PCB performs phase detection of the YIG-tuned oscillator's output frequency and provides a YIG loop error voltage to the A11 PCB.
- The A11 AM/FM PCB conditions the YIG loop error voltage, producing a correction signal that is sent to the A13 YIG Driver PCB. The YIG driver uses this signal to fine tune and phase lock the YIG-tuned oscillator. The A11 PCB also contains circuitry for FM modulation of the YIG-tuned oscillator.

Analog Instruction The A12 Analog Instruction PCB provides the frequency tuning voltages to the A13 YIG Driver PCB. It supplies band select information to the A9 or A9-1 PIN Control PCB, the A13 YIG Driver PCB, and the A14 Doubler Driver PCB or A14-1 SDM Driver PCB (for models with a frequency range greater than 20 GHz). The A17 CPU controls the A12 Analog Instruction PCB via the dedicated data and address bus.

YIG Driver The A13 YIG Driver PCB supplies the tuning current and bias voltages for the 2 to 20 GHz YIG-tuned oscillator. It also provides bias voltages for the 0.01 to 2 GHz Down Converter and the amplifiers located in the Switched Filter.

ALC/Square Wave Modulation This circuit subsystem consists of the A6 Square Wave Generator PCB, the A9 or A9-1 PIN Control PCB, the A10 ALC PCB, part of the A11 AM/FM Driver PCB, and the A14 Doubler Driver PCB (for models containing 20-40 GHz Frequency Extension Units). It provides level control of the RF output power, AM modulation, square wave modulation, and switch control and drive signals for the Switched Filter, the Frequency Extension Unit or Switched Doubler Module, and the Step Attenuator. The A17 CPU controls the A9 or A9-1 Pin Control PCB and the A10 ALC PCB via the dedicated data and address bus.

RF Deck This subsystem contains those elements related to the generation, modulation, and control of the sweep- and CW-frequency RF signals. These elements include; the 2 to 20 GHz YIG-tuned oscillator, the 0.01 to 2 GHz Down Converter, the Switched Filter, the 20 to 40 GHz Frequency Extension Unit or Switched Doubler Module, the Directional Coupler/ Level Detector, and the 110 dB Step Attenuator.

Power Supply The power supply subsystem consists of the A15 Regulator PCB, the A18 Power Supply PCB, the A19 Line Conditioner PCB, and part of the A21 Rear Panel PCB and Rear Casting Assembly. It supplies all the regulated DC voltages used by the sweep generator circuits via the A20 Motherboard PCB.

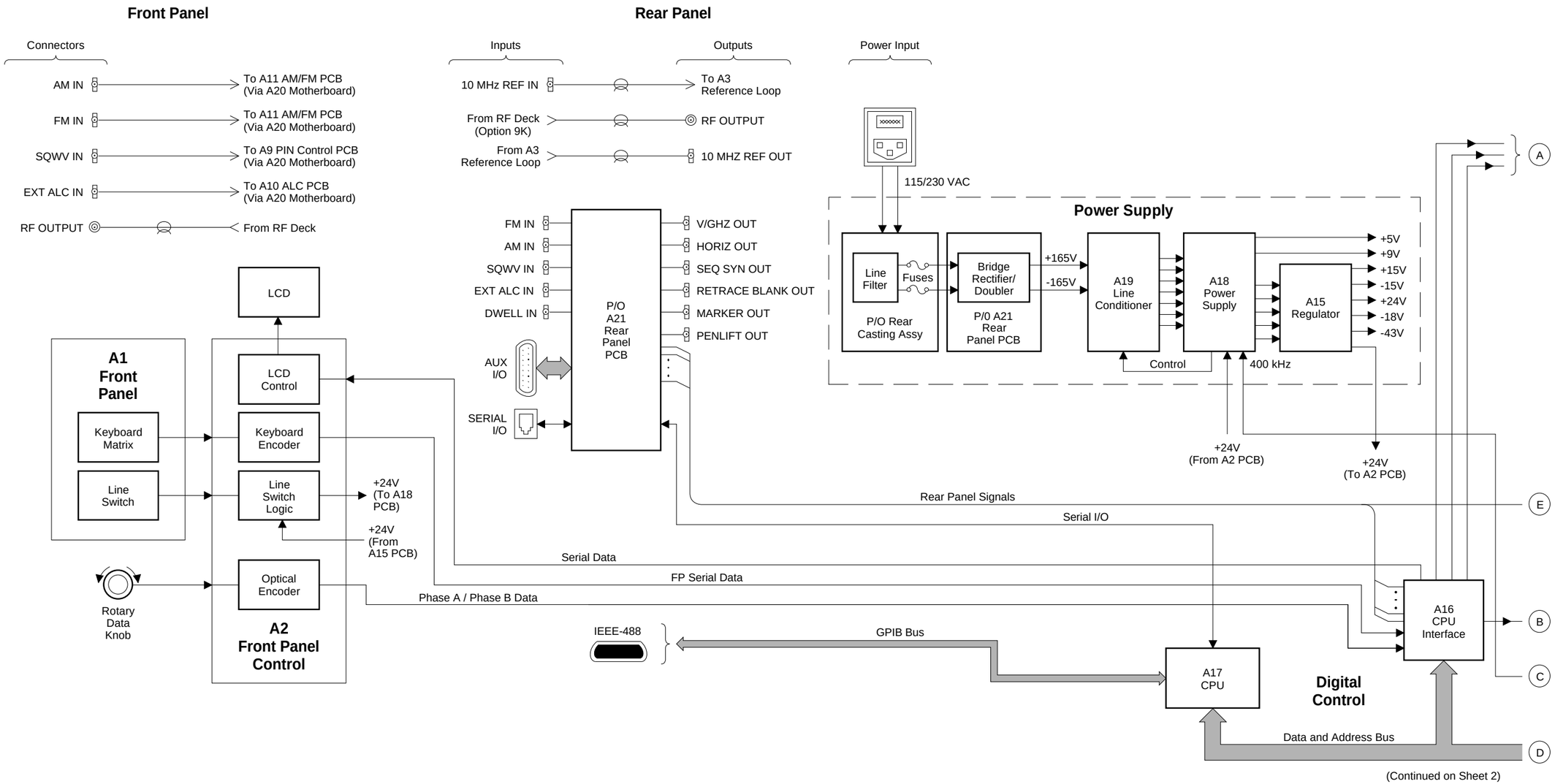


Figure 2-1. Block Diagram of a Typical 681XXA Synthesized Sweep Generator (Sheet 1 of 3)

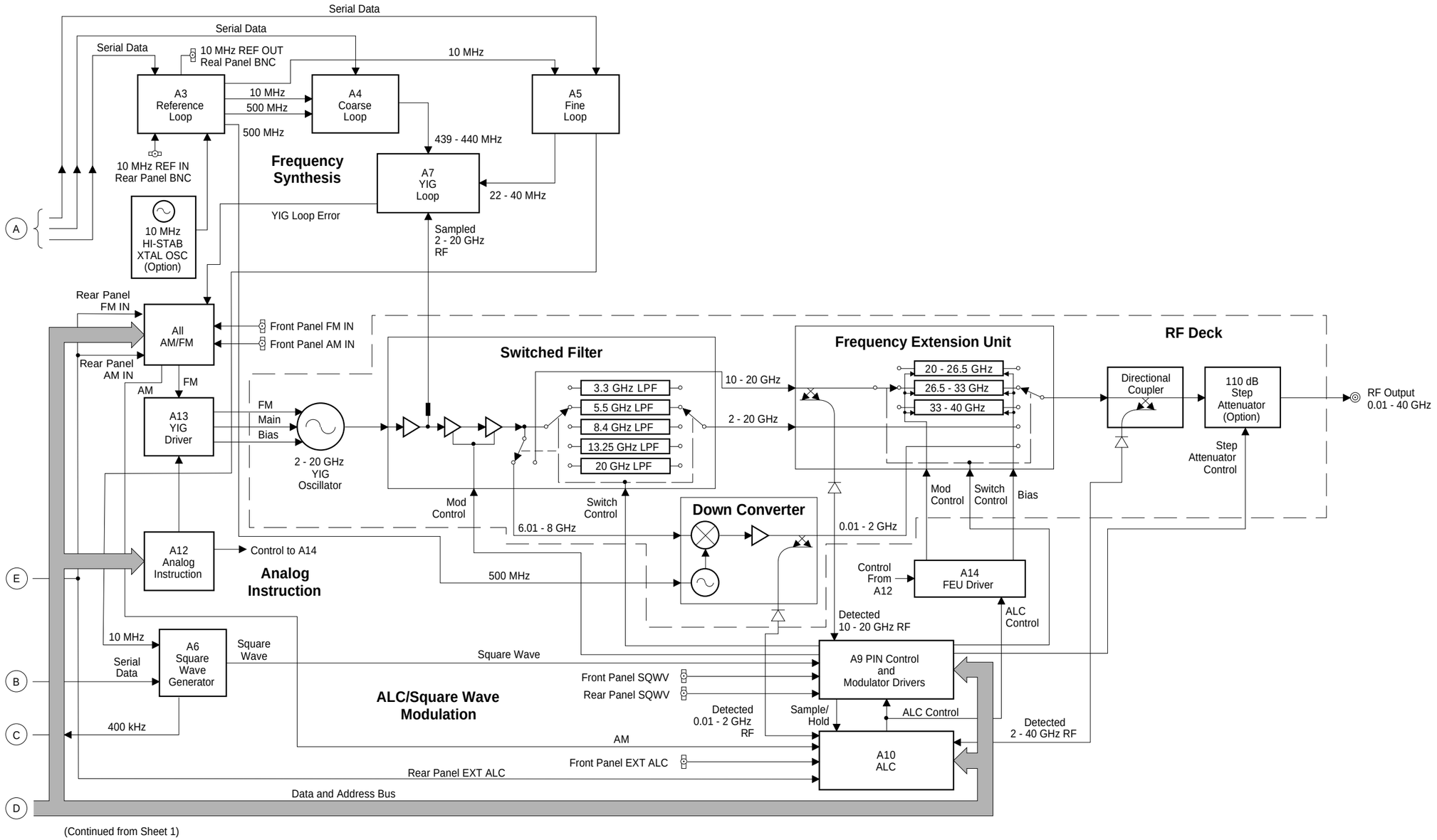


Figure 2-1. Block Diagram of a Typical 681XXA Synthesized Sweep Generator with the Frequency Extension Unit (Sheet 2 of 3)

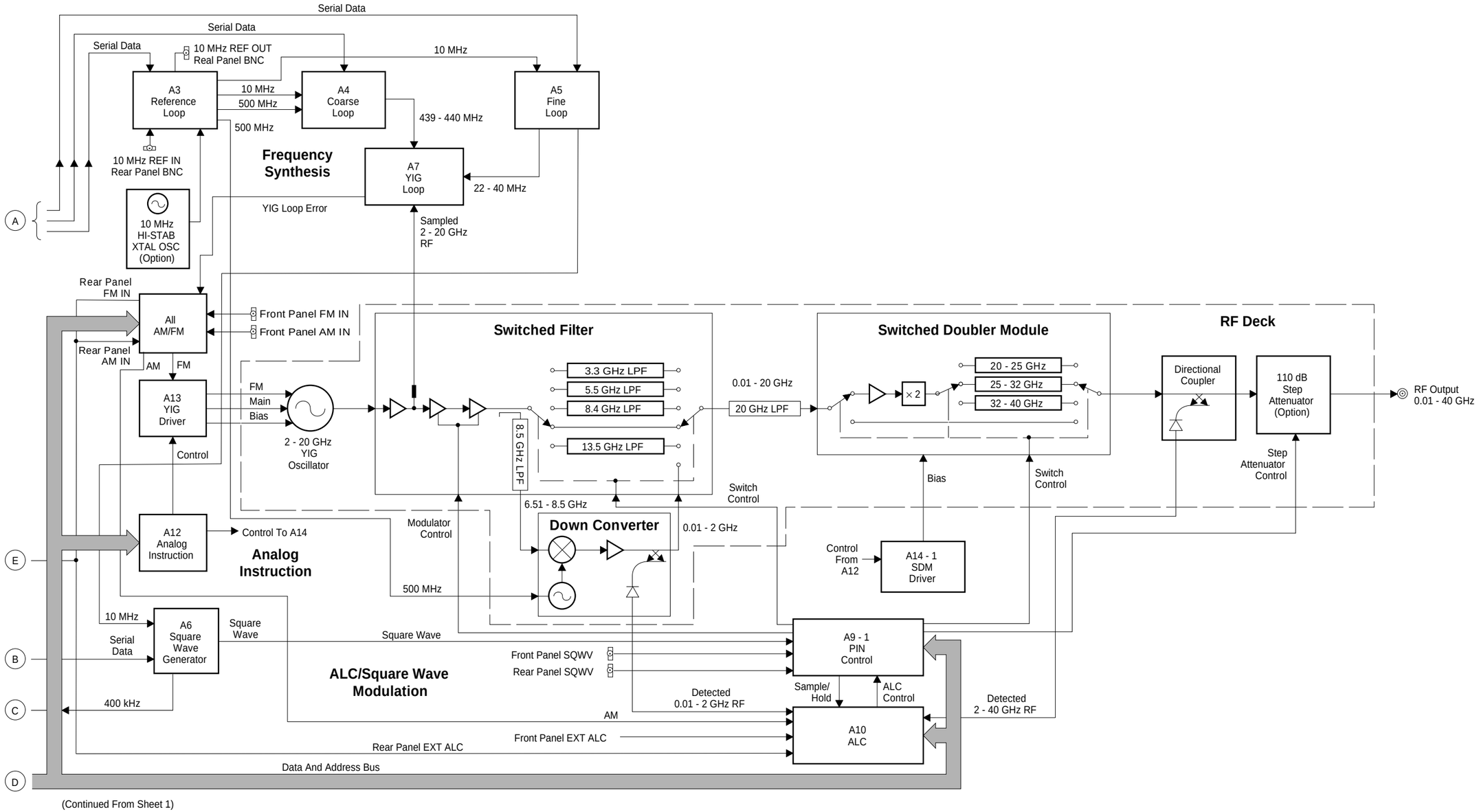


Figure 2-1. Block Diagram of a Typical 681XXA Synthesized Sweep Generator with the Switched Doubler Module (Sheet 3 of 3)

Inputs/ Outputs The A21 Rear Panel PCB and the A16 CPU Interface PCB contain the interface circuitry for the majority of the rear panel input and output connectors, including the AUX I/O connector. The front panel AM, FM, Square Wave, and External ALC inputs are routed via the A20 Motherboard PCB to the internal PCBs. The rear panel connectors, 10 MHz REF OUT and 10 MHz REF IN, are coupled directly to the A3 Reference Loop PCB via coaxial cables. The rear panel IEEE-488 GPIB and SERIAL I/O connectors are connected to the A17 CPU PCB via the A20 Motherboard PCB.

Motherboard/ Interconnections The A20 Motherboard PCB and associated cables provide the interconnections for the flow of data, signals, and DC voltages between all internal components and assemblies throughout the 681XXA.

2-3 FREQUENCY SYNTHESIS

The frequency synthesis subsystem provides phase-lock control of the sweep generator output frequency. It consists of four phase-lock loops, the Reference Loop, the Coarse Loop, the Fine Loop, and the YIG Loop. The four phase-lock loops, operating together, produce an accurately synthesized, low-noise RF output signal. Figure 2-2 (page 2-11) is an overall block diagram of the frequency synthesis subsystem. The following paragraphs briefly describe phase-lock loops and the overall operation of the frequency synthesis subsystem.

Phase Lock Loops The purpose of a phase-lock loop is to control the frequency of a variable oscillator in order to give it the same accuracy and stability as a fixed reference oscillator. It works by comparing two frequency inputs, one fixed and one variable, and supplying a correction signal to the variable oscillator to reduce the difference between the two inputs. For example, suppose we have a 10 MHz reference oscillator with a stability of 1×10^{-7}/day, and we wish to transfer that stability to a voltage controlled oscillator (VCO). The 10 MHz reference signal is applied to the reference input of a phase-lock loop circuit. The signal from the VCO is applied to the variable input. A phase detector in the phase-lock loop circuit compares the two inputs and determines whether the variable input waveform is leading or lagging the reference. The phase detector generates a correction signal that (depending on polarity) causes the VCO frequency to increase or decrease to reduce any phase difference. When the two inputs match, the loop is said to be *locked*. The variable input

from the VCO then equals the reference input in phase, frequency, accuracy, and stability.

In practical applications a frequency divider is placed between the output of the variable oscillator and the variable input to the phase-lock loop. The circuit can then be used to control a frequency that is an exact multiple of the reference frequency. In this way, the variable oscillator acquires the stability of the reference without equaling its frequency. In the A3 Reference Loop, the 100 MHz VCXO can be controlled by the phase-lock loop using a 10 MHz reference. This is because a divide-by-ten circuit is between the VCXO's output and the variable input to the phase-lock loop. Both inputs to the phase detector will be 10 MHz when the loop is locked.

If a programmable frequency divider is used, a number of frequencies can be phase-locked to the same reference. The limitation is that all must be exact multiples of the reference. The A4 Coarse Loop and A5 Fine Loop both use programmable frequency dividers.

Overall Operation

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of (1) its main tuning coil and (2) its FM (fine tuning) coil. Main tuning coil current from the YIG Driver PCB coarsely tunes the YIG-tuned oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop is then used to fine tune the YIG-tuned oscillator to the exact output frequency and to reduce FM noise close to the carrier.

One input to the YIG Loop is the 439 to 490 MHz signal from the Coarse Loop. This signal is divided by two and then amplified to drive the step-recovery diode. The step-recovery diode produces harmonics of the coarse loop signal (≥1.9755 to ≈20 GHz). These harmonics are used by the sampler.

The other input to the sampler is the RF output signal from the YIG-tuned oscillator. Mixing this RF output signal sample with the adjacent coarse-loop harmonic produces a low frequency difference signal that is the YIG IF signal (22 to 40 MHz).

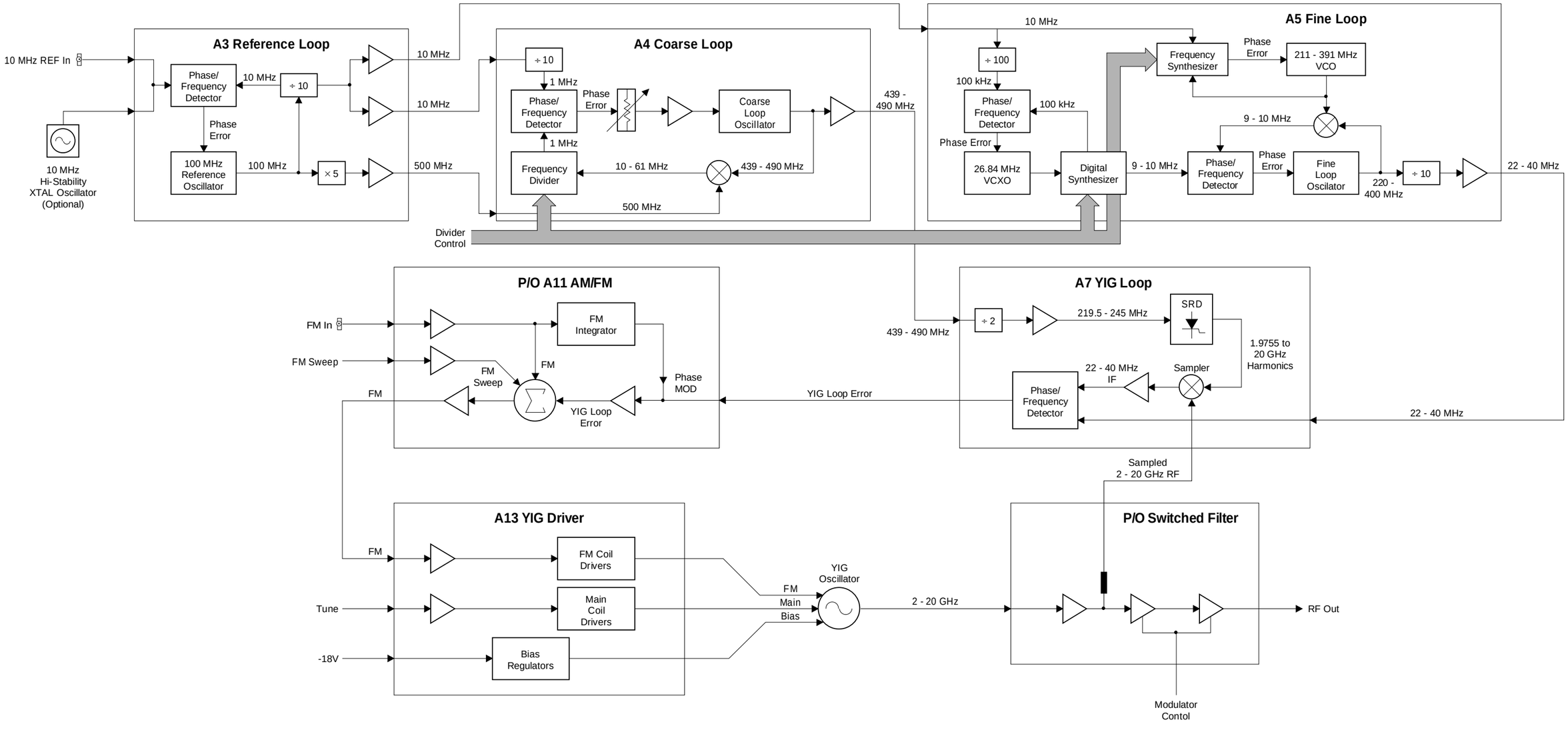


Figure 2-2. Block Diagram of the Frequency Synthesis Subsystem

The sweep generator's CPU programs the coarse-loop oscillator's output frequency so that one of its harmonics will be within 22 to 40 MHz of the desired YIG-tuned oscillator's output frequency. The YIG Loop phase detector compares the YIG IF signal to the 22 to 40 MHz frequency reference signal from the Fine Loop. If there is a difference, the YIG phase detector fine tunes the YIG-tuned oscillator (via the FM circuitry and the FM coil drivers) to eliminate any frequency difference between the two signals.

Table 2-1. *RF Output and Loop Frequencies*

RF OUTPUT/LOOP FREQUENCIES (in MHz)		
RF OUT	**COARSE LOOP**	**FINE LOOP**
2000	439	24.5
3000	458	23
4000	468	22
5000	474	23
6000	478	25
7000	481	25.5
8000	483	30.5
9000	485	27.5
10000	486	37
11000	477	29
12000	479	25

Phase locking the sweep generator's output frequency over a broad frequency range is accomplished by programming the coarse-loop oscillator's output to various frequencies that have harmonics close to desired operating frequencies. Exact frequency tuning for each desired operating frequency is accomplished by programming the fine-loop oscillator. (In each case, the YIG-tuned oscillator is first tuned via the main tuning coil to the approximate desired operating frequency.) Table 2-1 shows the coarse-loop and fine-loop frequencies for specific RF output frequencies.

The coarse-loop oscillator has a programming (tuning) range of 439 to 490 MHz and a resolution of 1 MHz. This provides harmonics between ≥1.9755 and approximately 20 GHz. This allows any YIG-tuned oscillator output frequency to be down converted to a YIG IF signal of 22 to 40 MHz.

The YIG Loop is fine tuned by varying the 22 to 40 MHz reference frequency signal applied to the YIG loop phase detector. By programming the fine-loop oscillator, this signal can be adjusted in 1 kHz increments over the 22 to 40 MHz range. The resolution of the fine-loop oscillator (hence the resolution of the RF output signal) is 1 kHz, which is much finer than is available from the coarse loop alone. For applications requiring a resolution finer than 1 kHz, an optional tuning resolution of 0.1 Hz is available.

The Coarse Loop and Fine Loop outputs are derived from high-stability 10 MHz and 500 MHz signals generated by the Reference Loop. For applications requiring even greater stability, the 100 MHz reference oscillator can be phase locked to an optional 10 MHz reference (internal or external).

RF Outputs 0.01 to 40 GHz

Refer to the block diagram of the RF Deck shown in Figure 2-1 for the following description. The 681XXA uses one 2 to 20 GHz YIG-tuned oscillator. All other frequencies output by the sweep generator are derived from the fundamental frequencies generated by this YIG-tuned oscillator.

RF output frequencies of 0.01 to 2 GHz are developed by down converting the fundamental frequencies of 6.01 to 8 GHz. This is achieved using a 6.0 GHz local oscillator signal that is phase locked to the 500 MHz output of the Reference Loop. Precise control of the 0.01 to 2 GHz frequencies to 1 kHz accuracy is accomplished by phase-lock control of the 6.01 to 8 GHz fundamental frequencies prior to down conversion.

RF output frequencies of 20 to 40 GHz are produced by doubling of the fundamental frequencies of 10 to 20 GHz. Phase-lock control of the 10 to 20 GHz fundamental frequencies, accomplished prior to doubling, ensures precise control of the 20 to 40 GHz frequencies to 1 kHz resolution.

Frequency Modulation

Frequency modulation (FM) of the YIG-tuned oscillator RF output by external signals is performed by summing the external signals into the FM control path of the YIG loop. Refer to Figures 1-1 and 1-2. FM inputs from the front panel and rear panel are routed via the A20 Motherboard PCB to the FM amplifier circuits located on the A11 AM/FM PCB. These circuits frequency modulate the RF output signal by controlling the YIG-tuned oscillator's FM (fine tuning) coil current.

Sweep Mode of Operation

Broad-band analog sweeps (>100 MHz wide) of the YIG-tuned oscillator RF output are accomplished by applying appropriate analog sweep ramp signals, generated by the A12 Analog Instruction PCB, to the YIG-tuned oscillator's main tuning coil (via the A13 YIG Driver PCB). In this mode, the start, stop, and bandswitching frequencies are phase-lock-corrected during the sweep.

Narrow-band analog sweeps (≤100 MHz wide) of the YIG-tuned oscillator RF output are accomplished by summing appropriate analog sweep ramp signals, generated by the A12 Analog Instruction PCB, into the YIG-tuned oscillator's FM tuning coil control path. The YIG-tuned oscillator's RF output is then

swept about a center frequency. The center frequency is set by applying a tuning signal (also from the A12 PCB) to the YIG-tuned oscillator's main tuning coil (via the A13 YIG Driver PCB). In this mode, YIG loop phase locking is disabled except during center frequency correction, which occurs during sweep retrace.

Digital (step) sweeps of the YIG-tuned oscillator RF output consist of a series of discrete, synthesized steps between a start and stop frequency. Each frequency step is generated by applying the tuning signal (from the A12 Analog Instruction PCB) to the YIG-tuned oscillator's main tuning coil, then phase-locking the RF output. Every frequency step in the sweep range is phase-locked.

2-4 ALC AND MODULATION

The ALC and modulation subsystem provides automatic level control (ALC), amplitude modulation (AM), and square wave modulation of the RF output signal. The ALC loop consists of circuits located on the A10 ALC PCB, the A9 or A9-1 PIN Control PCB, and the A14 Doubler Driver PCB (for models containing 20-40 GHz Frequency Extension Units). These circuits interface with the modulators and the Directional Coupler/Level Detector components on the RF deck. AM modulation circuits (located on the A11 AM/FM Driver PCB and A10 ALC PCB) are included in this loop.

Square wave modulation of the RF output signal is provided by circuits located on the A6 Square Wave Generator PCB and the A9 or A9-1 PIN Control PCB. The overall block diagram of the ALC and modulation subsystem is shown in Figure 2-3. The following paragraphs briefly describe the operation of the subsytem components.

ALC Loop Operation

In the 681XXA, a portion of the RF output is detected and coupled out of the Directional Coupler/Level Detector as the feedback input to the ALC loop. The feedback signal from the detector is routed to the A10 ALC PCB where it is compared with a *reference voltage* that represents the desired RF power output level. If the two voltages do not match, an error correction signal is fed from the A10 ALC PCB to the modulator shaper amplifier circuit located on the A9 or A9-1 PIN Control PCB. The resulting ALC control voltage output causes the modulator, located in the Switched Filter, to adjust the RF output level. Thus, the feedback signal from the detector will be set equal to the reference voltage.

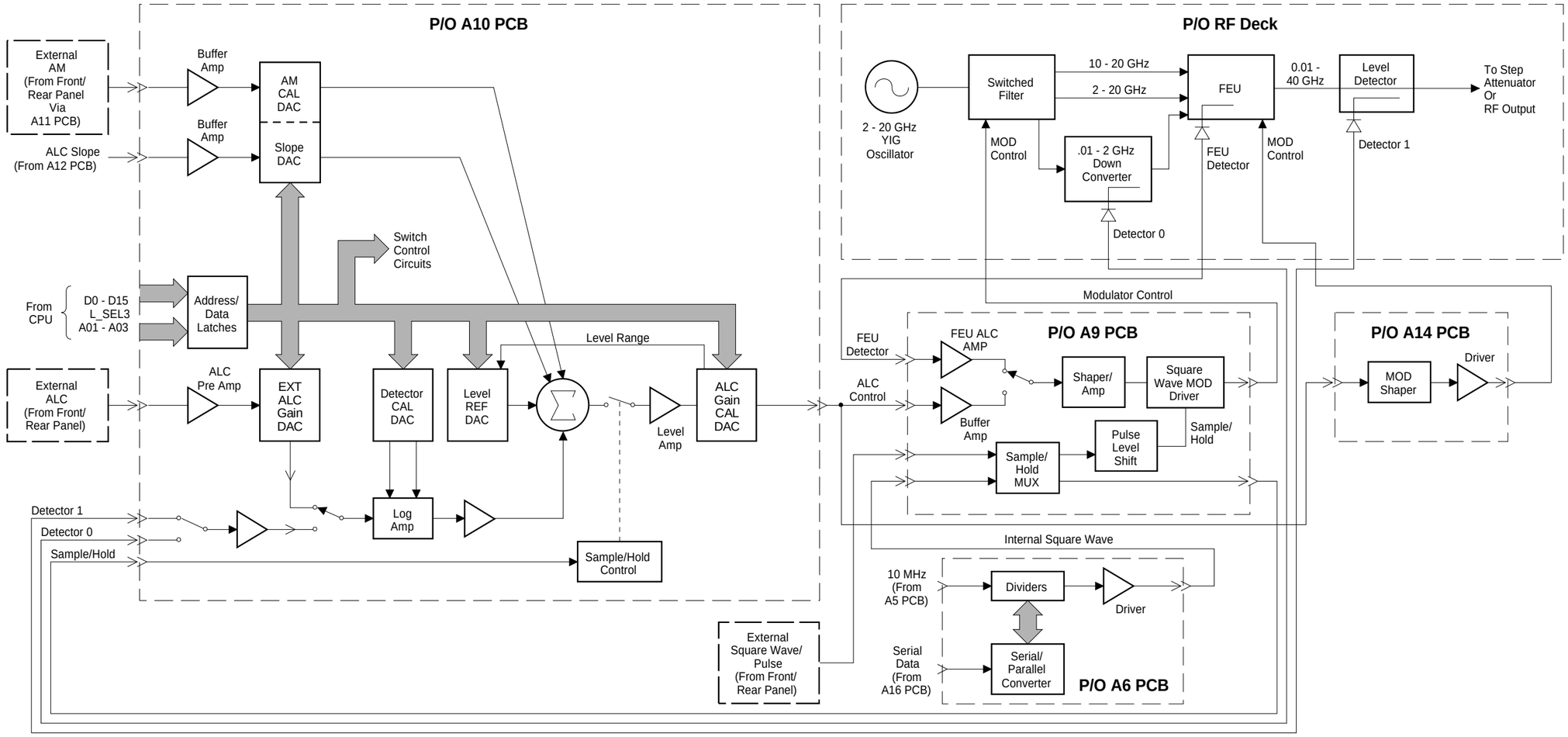


Figure 2-3. Block Diagram of the ALC and Modulation Subsystem

For models containing Frequency Extension Units (FEU), modulators in the FEU control the RF power output level for the 20 to 40 GHz portion of the frequency range. The error correction signal from the A10 ALC PCB is fed to the modulator shaper/driver circuits located on the A14 Doubler Driver PCB. The resulting ALC control voltage output causes the modulators, located in the FEU, to adjust the RF output level. To prevent overloading the FEU doublers, a portion of the 10 to 20 GHz RF input is detected and sent to the modulator shaper amplifier circuit on the A9 PIN Control PCB. The resulting ALC control voltage causes the Switched Filter modulator to adjust the FEU RF input to required levels.

NOTE

The sweep generator uses two internal level detection circuits. For frequencies <2 GHz, the level detector is part of the Down Converter. The signal from this detector is routed to the A10 ALC PCB as the Detector 0 input. For frequencies ≥2 GHz, the level detector is part of the main Directional Coupler. The signal from this detector is routed to the A10 ALC PCB as the Detector 1 input.

The Level Reference DAC, under the control of the CPU, provides the RF level reference voltage. By setting the output of this DAC to the appropriate voltage, the CPU adjusts the RF output power to the level selected by the user. The desired RF output level may be set over a 28 dB range (standard) using front panel controls or the GPIB. For those units with the optional 110 dB step attenuator, the RF output level range is 0 to 135 dB.

External Leveling

In the external leveling mode, an external detector monitors the RF output level of the sweep generator instead of an internal level detector. The external detector output goes to the A10 ALC PCB from the front or rear panel inputs. The ALC controls the RF power output level as previously described.

Power Sweep
In this mode, the CPU has the ALC step the RF output through a range of levels specified by the user. This feature can be used in conjunction with the sweep mode to produce a set of identical frequency sweeps, each with a different RF power output level.

Amplitude Modulation
Amplitude modulation (AM) of the RF output signal by external signals is accomplished by summing the external signals into the ALC loop. AM inputs from the front panel and rear panel are routed to the AM input circuitry on the A11 AM/FM Driver PCB. After processing, the AM signal goes to the A10 ALC PCB, where it is summed with the level reference and detector inputs into the ALC loop. The ALC control signal is therefore modulated by the AM input waveform. The action of the ALC loop then causes the envelope of the RF output signal to track the external modulation signal.

Square Wave Modulation

Square wave modulation is accomplished by turning the RF output signal on and off using internally generated square wave or external square wave inputs.

The A6 Square Wave Generator PCB, under control of the CPU, divides the 10 MHz reference signal received from the A5 Fine Loop PCB to produce square waves. These internal square wave signals are fed to the A9 or A9-1 PIN Control PCB. There they are multiplexed with the external square wave signals received from the front or rear panel. The output of the multiplexer is two sample/hold signals. One goes via pulse level shift circuitry to the ALC modulator driver to modulate the RF output signal; the other goes to the A10 ALC PCB to cause the level amplifier to operate as a sample/hold amplifier. The amplifier is synchronized with the modulating signal so that the ALC loop effectively operates only during the *ON* portion of the modulated RF output signal.

2-5 A1 AND A2 FRONT PANEL PCBs

The A1 Front Panel and A2 Front Panel Control PCBs are part of the Front Panel subsystem (Figure 2-4). These PCBs, which are mounted within the front panel casting, contain circuits that perform the following functions:

- Provide front panel controls for operator inputs to the CPU.
- Interface the front panel LCD, LEDs, and controls with the CPU via the serial data bus.

The A1 Front Panel PCB is mounted on the rear surface of the front panel and contains the conductive rubber key switches and LEDs for the front panel. The key switches are configured as double-pole, single-throw switches. The contacts of each switch are a part of the etching on the component side of the PCB. Pressing the front panel key cap flexes the conductive-rubber switch membrane and forces it into contact with the PCB traces, thus closing the switch. The front panel has four LEDs—STANDBY, OPERATE, RF ON, and RF OFF. The key switch interface circuits and LED control circuits are contained on the A2 Front Panel PCB.

The A2 Front Panel Control PCB interfaces the CPU via the serial data bus to the front panel LCD, LEDs, and controls. The main circuit blocks on this PCB are:

- Serial interface
- LCD control
- Keyboard interface
- Line switch logic
- Optical encoder

Serial Interface

The CPU sends data to the front panel subsystem via the A16 CPU Interface PCB in a 16-bit serial data word format. (The lower eight bits contains the data and the upper eight bits contain the destination address of the data.) The serial data word is clocked into the serial-to-parallel converter by the front panel clock signal. Upon completion of the 16-bit data transfer, the front panel strobe signal enables the strobe decoder to load the data into the appropriate parallel data latch.

Pressing a key on the front panel causes a keyboard interrupt to go to the CPU. Upon receiving the interrupt, the CPU sets up the serial interface on the A16 PCB and clocks the keycode data out of the parallel-to-serial converter to the A16 PCB. The CPU then reads this data and takes appropriate action.

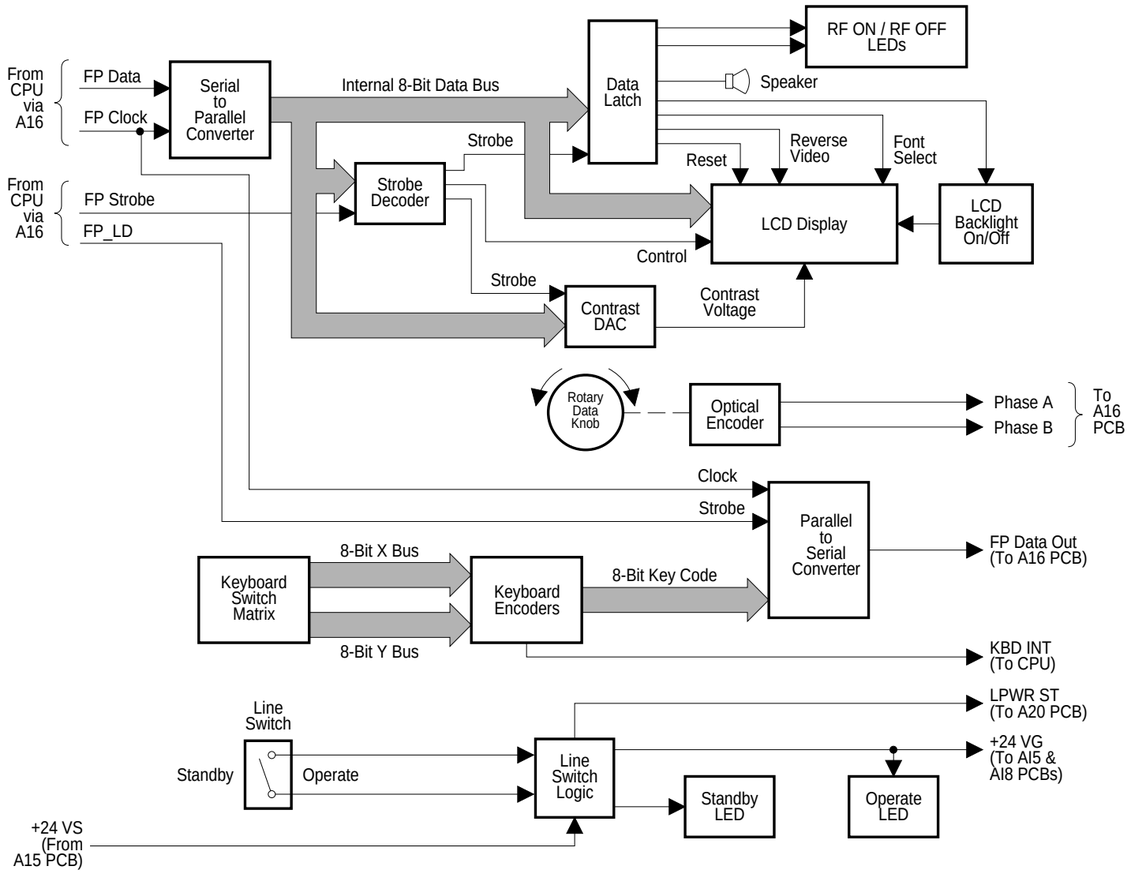


Figure 2-4. Overall Block Diagram of the Front Panel Subsystem

LCD Control

The front panel Liquid Crystal Display (LCD) has its own built in controller and can display 8 lines of 40 characters each. The Control line from the strobe decoder controls the data flow to the LCD controller. (When the line is set high, the data is a command to the controller; when the line is set low, the information is data.)

The Contrast DAC supplies –5.5V to –11.5V to the LCD to control the contrast of the display. The user may adjust this DAC, via the system menu, to compensate for changing ambient light conditions. A strobe from the strobe decoder latches the data into the Contrast DAC.

Other LCD control signals are received via the Data Latch. The Reset signal resets the LCD controller on power up and instrument preset; the Reverse Video signal selects standard or reverse video display; and the control signal to the LCD backlight circuit selects display backlight on or off. In addition to LCD control signals, the Data Latch also controls the RF ON and RF OFF LEDs and the front panel speaker.

Keyboard Interface

All of the key switches on the A1 PCB, except for the LINE key, are connected into a matrix consisting of eigth X-lines and eight Y-lines. Closing a key switch connects its X and Y coordinate lines to ground. The keyboard encoder circuits convert the X and Y coordinates into a 8-bit, parallel keycode signal. These circuits also generate an interrupt signal, KBD INT, which goes via the A16 PCB to the CPU.

When the CPU detects the keyboard interrupt, it sets up the serial interface on the A16 PCB and sends FP_LD to strobe the parallel keycode data into the parallel-to-serial converter. The clock signal then shifts the keycode data out serially to the A16 PCB. The CPU reads the data and takes appropriate action. In addition to loading the keycode data into the converter, the strobe signal, FP_LD, also clears the keyboard interrupt.

Line Switch Logic

The 681XXA is configured with the L PWR ST line grounded on the A20 Motherboard PCB. This configuration causes the sweep generator to come up in the Operate mode anytime it is connected to line voltage. The +24 volts received from the standby

regulator provides power to the line switch logic circuitry. This activates the line switch relay to supply +24 volts to the OPERATE LED and the A15 Regulator and A18 Power Supply PCBs. Pressing the front panel LINE key deactivates the line switch relay. This removes the +24 volts from the A15 and A18 PCBs and applies it to the STANDBY LED.

Optical Encoder

The front panel Rotary Data Knob lets the operator modify the value of parameters that have been previously entered. It controls the optical encoder, which produces Phase A and Phase B signals as the knob is turned. The direction of rotation determines the phase relationship between these two signals; the rate of rotation determines their frequency. The Phase A and Phase B signals go to the A16 CPU Interface PCB, where they are processed into parallel data that can be read by the CPU. The CPU will only read this data when a parameter is open for editing.

2-6 A3 REFERENCE LOOP PCB

The A3 Reference Loop PCB (Figure 2-5) provides the stable 10 MHz and 500 MHz reference frequency signals that are used throughout the sweep generator for phase locking.

Reference Loop Oscillator

The reference loop oscillator is a 100 MHz oven-controlled crystal oscillator (OCXO) that can be tuned over a very narrow range with a DC voltage. The oven stabilizes the oscillator's frequency over temperature by keeping the crystal at a constant temperature with changing ambient conditions.

The oscillator's control signal input permits fine frequency adjustment of the 100 MHz. When the instrument is powered on, oscillator calibration data, stored in non-volatile memory during calibration, is sent by the CPU to the reference loop via the A16 CPU Interface PCB. The serial data is clocked in and converted to parallel data. It is then strobed into the 100 MHz CAL DAC. The calibration signal from the DAC is amplified, then goes to the control signal input to tune the oscillator to exactly 100 MHz. This control signal input also allows the oscillator to be phase locked to a 10 MHz reference.

Reference Frequency Outputs

The 100 MHz output from the oscillator has two paths. In one path, the signal is multiplied by five and filtered to generate a 500 MHz output. This signal is buffered and sent to the A4 Coarse Loop PCB and the 0.01 to 2 GHz Down converter. The 500 MHz signal output levels are +5 dBm ±5 dB.

In the other 100 MHz output path, the signal is divided by ten to produce a 10 MHz output. This signal is buffered and sent to the A4 Coarse Loop PCB, the A5 Fine Loop PCB, and the Rear Panel 10 MHz REF OUT BNC connector. These 10 MHz signal output levels are +3 dBm ±3 dB. A 10 MHz signal from the divider also goes to the phase/frequency detector as the variable input during oscillator phase lock (described in the next paragraph).

Oscillator Phase Locking

If better time base stability is desired, the reference loop oscillator can be phase locked to either an optional internal high-stability 10 MHz crystal oscillator (Option 16) or an external 10 MHz reference signal. The control logic circuitry automatically senses the presence of a 10 MHz reference and switches in the phase/frequency detector. The switching control logic prioritizes the available refer-

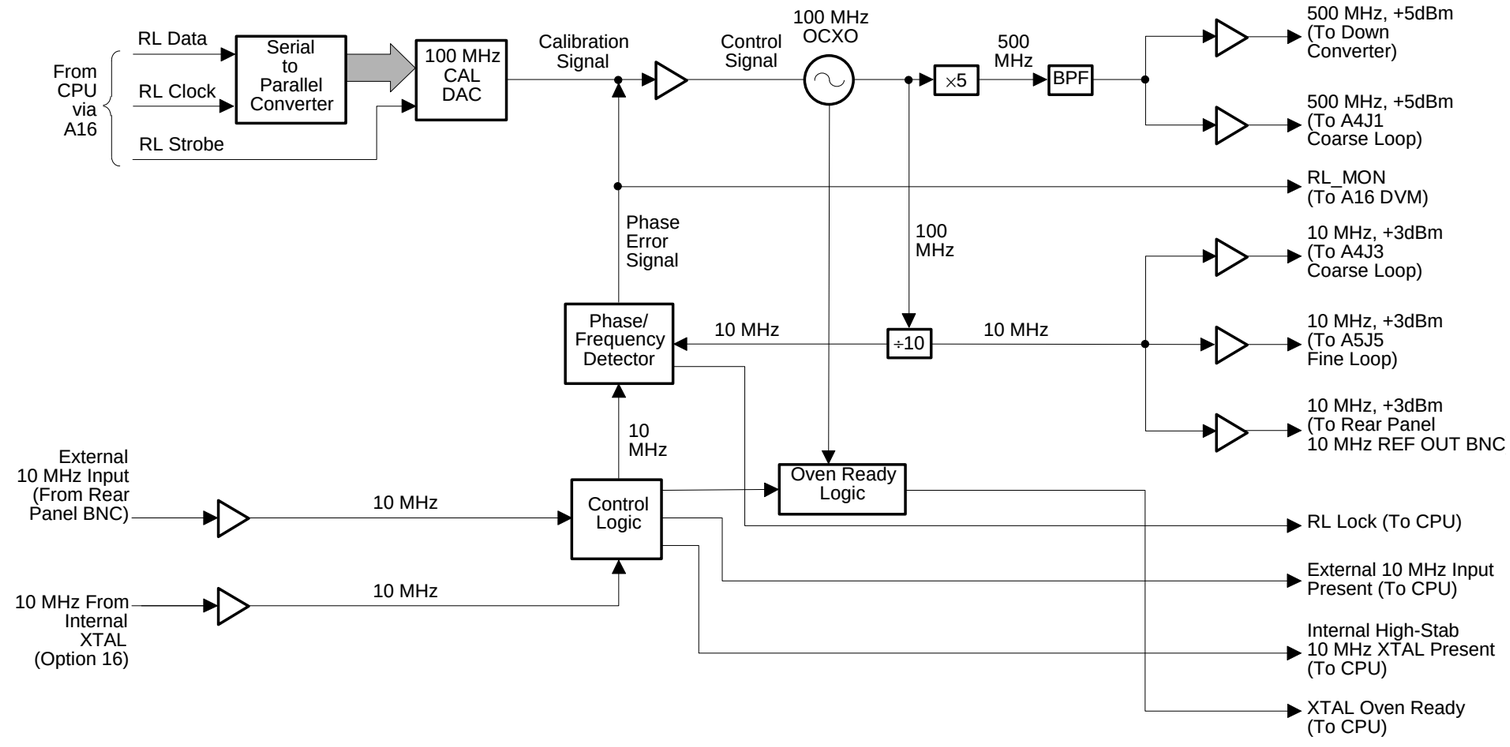


Figure 2-5. Block Diagram of the A3 Reference Loop PCB

ences and gives top priority to the external 10 MHz reference.

The phase/frequency detector compares the 10 MHz reference signal input to the 10 MHz variable signal input (from the reference loop oscillator). If there is a difference between the inputs, the detector generates an error signal. The phase error signal is amplified by the loop amplifier and fed to the 100 MHz oscillator to phase lock it to the 10 MHz reference. The phase-lock loop has a bandwidth of approximately 30 Hz. The bandwidth is kept low so that the phase noise of the instrument is not degraded by a noisy external reference.

Reference Loop Monitoring

The reference loop generates various signals that can be used to monitor its status. Status signals are sent to the CPU to indicate that (1) the crystal oven has reached operating temperature, (2) an external 10 MHz reference has been applied, (3) the optional internal high-stability 10 MHz time base is installed, and (4) the reference loop is phase locked to a 10 MHz reference. The signal RL_MON (loop phase error signal) goes to the DVM circuitry on the A16 PCB for use in calibration and testing.

2-7 A4 COARSE LOOP PCB

The A4 Coarse Loop PCB (Figure 2-6 on page 2-27) generates the 439 to 490 MHz coarse tuning frequency used by the YIG loop to phase lock the sweep generator.

Coarse Loop Oscillator

The coarse loop oscillator is a voltage-controlled oscillator (VCO) that covers the 439 to 490 MHz range. The resolution of the coarse loop is 1 MHz and the oscillator's output is phase locked to the 10 MHz reference frequency from the A3 Reference Loop PCB.

The 439 to 490 MHz output of the oscillator has two paths. In one path, the signal is buffered and sent to the A7 YIG Loop PCB. The signal output level is 4 dBm ±5 dB. In the other output path, the signal is fed to the coarse loop mixer.

Coarse Loop Mixer/IF

The 439 to 490 MHz signal from the coarse loop oscillator goes via a buffer, a 16 dBm attenuator, and a second buffer to the RF input of the coarse loop mixer. The alternating buffer/attenuator configuration is used to provide good isolation from the mixer input to the oscillator output. This additional isolation prevents other frequencies present in the mixer from leaking back into other circuits.

The 500 MHz local oscillator input to the mixer comes from the A3 Reference Loop PCB via a buffer. The 439 to 490 MHz output of the coarse loop oscillator is mixed with the 500 MHz local oscillator signal to produce a 10 to 61 MHz IF. The output level of the IF signal is –6 dBm.

The IF signal passes through a 80 MHz low-pass filter that removes any undesirable products of the mixing process. The filtered IF signal then goes to the IF amplifier/limiter circuitry. Limiting prevents any AM component on the IF signal from causing an FM component in the phase detector output signal (which would degrade the phase noise performance of the oscillator). The IF signal is converted to a TTL compatible level for input to the frequency dividers.

Coarse Loop Dividers

The IF signal goes to the frequency divider circuits where it is divided down to 1 MHz. The programmable frequency dividers are high speed (100 MHz) TTL dividers. The divider number to be loaded into the frequency dividers is received from the CPU via

the serial interface. The 1 MHz signal output from the dividers goes to the phase/frequency detector.

Oscillator Pre-Tuning

The coarse loop oscillator is tuned close to the correct output frequency by the pre-tune DAC, then phase locked by the phase-lock loop. The use of the pre-tune DAC speeds up the tuning of the oscillator which reduces lock acquisition time. It also lets the loop operate at close to 0 volts when locked, thus allowing maximum signal swing for improved acquisition. The pre-tune DAC receives its tuning information from the CPU via the serial interface. During frequency change, the loop is momentarily opened which lets the pre-tune DAC set the new oscillator frequency without loop interference.

Oscillator Phase Locking

The 10 MHz reference signal, received from the A3 Reference Loop PCB, is first divided by ten then fed to the phase/frequency detector, where it is compared to the 1 MHz signal from the frequency dividers. If a difference exists, the detector generates a phase-error signal which goes to the loop amplifier. Whenever the loop is phase locked, the detector sends a lock signal to the CPU.

From the loop amplifier, the phase-error signal goes to a gain compensation network. Loop gain compensation is needed to maintain a nearly constant loop bandwidth at all tuning frequencies. This results in a much more stable loop. Control of the gain compensation network is accomplished using the same data as the frequency dividers. This makes the amount of gain compensation directly related to the divider number. The phase-error signal output from the gain compensation network is summed with the output of the pre-tune DAC to provide the tuning voltage for the coarse loop oscillator.

The loop phase-error signal output of the loop amplifier also goes as signal CL_MON to the DVM circuitry on the A16 PCB. There it is used in calibration and testing.

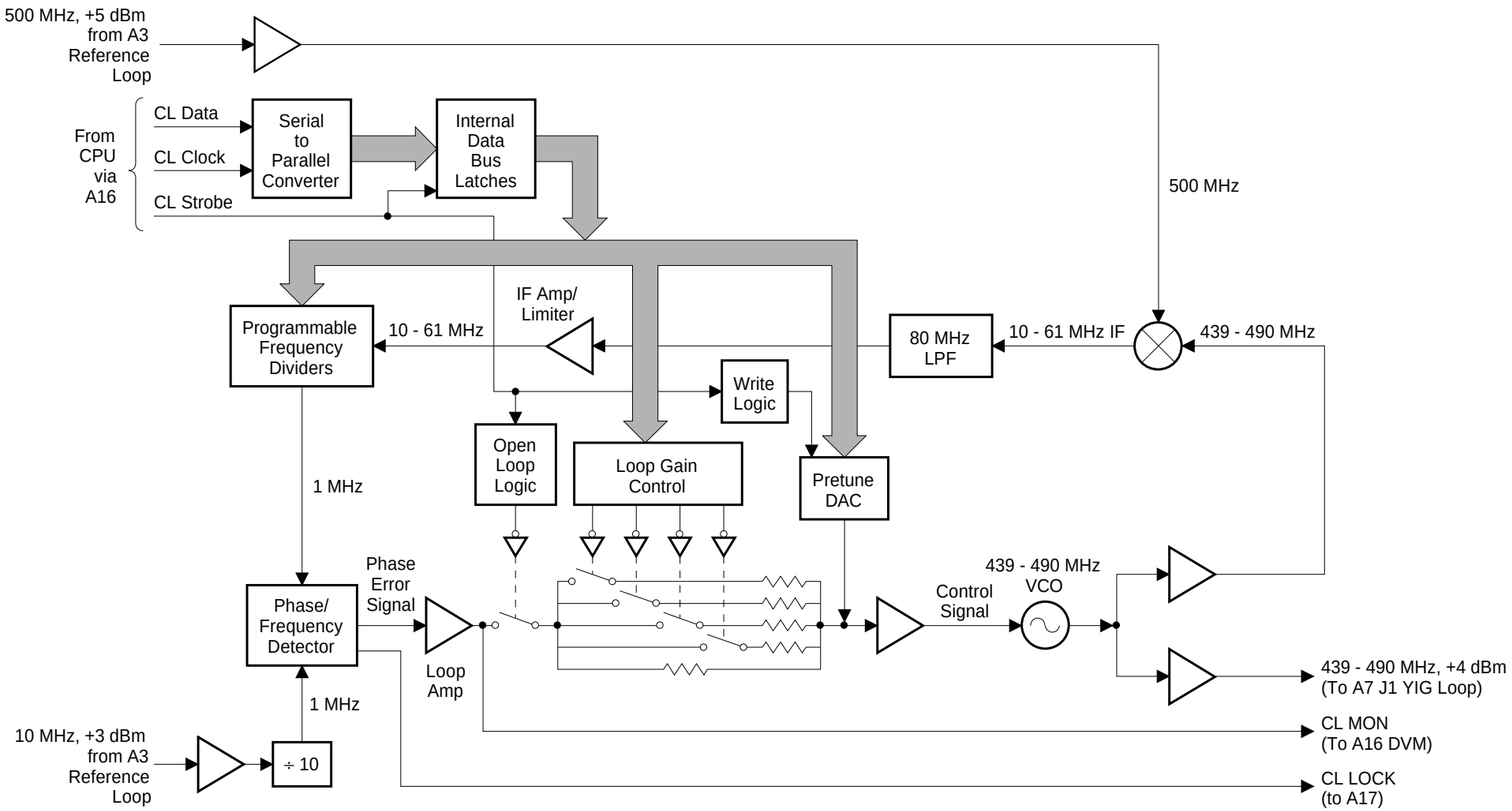


Figure 2-6. Block Diagram of the A4 Coarse Loop PCB

Serial Interface

The CPU sends tuning and divider control data to the coarse loop via the A16 PCB in a 16-bit serial data word format. The serial data word is clocked into the serial-to-parallel converter by the coarse loop clock signal. Upon completion of the 16-bit data transfer, the coarse loop strobe signal loads the data into the internal parallel data bus latches. The strobe also triggers the logic circuits that write the tuning data to the pre-tune DAC and momentarily opens the loop during oscillator tuning.

2-8 A5 FINE LOOP PCB

The A5 Fine Loop PCB (Figure 2-7 on page 2-31) provides the 22 to 40 MHz fine tuning reference frequencies used by the YIG loop to phase lock the sweep generator.

Fine Loop Oscillator

The fine loop oscillator is a voltage-controlled oscillator (VCO) that covers the 220 to 400 MHz range. The resolution of its output is 6.25 mHz (0.00625 Hz). This fine frequency resolution is achieved by phase locking the oscillator's output to a 9 to 10 MHz reference frequency from a Direct Digital Synthesizer (DDS).

The output of the fine loop oscillator is split into two paths. In one path, the signal is divided by ten, buffered, and sent to the A7 YIG Loop PCB. This is the 22 to 40 MHz fine tuning frequency output. It has a resolution of 625 µHz (0.000625 Hz) and an output level of 3 dBm. In the other output path, the signal is fed to the fine loop mixer.

Fine Loop Mixer/IF

The 220 to 400 MHz signal from the fine loop oscillator goes via a buffer, a 16 dBm attenuator, and a second buffer to the RF input of the fine loop mixer. This buffering and attenuating isolates the fine loop output from the fine loop mixer.

The local oscillator input to the mixer comes from the 211 to 391 MHz VCO. The RF and local oscillator mixer inputs are offset by 9 to 10 MHz, so that the mixer produces a 9 to 10 MHz IF. The output level of the IF signal is –6 dBm.

The IF signal goes through a 50 MHz low-pass filter then on to the IF limiter/amplifier. Limiting prevents any AM component on the IF signal from causing an FM component in the phase detector output signal (which would degrade the phase noise performance of the fine loop oscillator). The IF signal is converted to a TTL level for input to the fine loop phase/frequency detector.

Local Oscillator Loop

The 211 to 391 MHz VCO generates the local oscillator signal for the fine loop mixer. The output of this oscillator is split into two paths. In one path, the signal is buffered and fed to the fine loop mixer. In the other path, the signal is buffered and sent to the frequency synthesizer.

The frequency synthesizer contains programmable frequency dividers and a phase/frequency detector. In addition to the VCO input, it receives frequency divider programming data and a 10 MHz reference input. The CPU sends the numbers to be loaded into the frequency dividers via the serial interface.

The phase/frequency detector reference frequency is 1 MHz. Therefore, the divider ratio for the reference input is 10 and the divider ratio for the VCO input is 211 to 391. The phase/frequency detector compares the 1 MHz inputs and generates an error voltage. This loop error voltage goes to the VCO to tune it to the correct output frequency.

10 MHz Reference Input

The 10 MHz reference signal input to the A5 PCB comes from the A3 Reference Loop PCB. It provides a reference for loops on the A5 PCB. It also goes, via a buffer, to the A6 Square Wave Generator PCB. The 10 MHz signal is converted to TTL levels. Then it is fed to the divider and, through a buffer, to the frequency synthesizer IC. The 10 MHz signal is divided by 100 to provide a 100 kHz reference for the reference loop phase/frequency detector.

Reference Loop

The reference loop consists of the voltage-controlled crystal oscillator (VCXO), the DDS, a phase/frequency detector, and associated circuitry. The VCXO provides the clock frequency of 26.8435456 MHz for the DDS. The DDS has a 32-bit wide phase accumulator that, when driven by the clock frequency, produces a minimum output resolution of 6.25 mHz (0.00625 Hz). The DDS produces two outputs—a 100 kHz signal to phase lock the VCXO and a 9 to 10 MHz reference signal for phase locking the fine loop. The CPU sends data for programming the DDS via the serial interface.

The 100 kHz signal output from the DDS goes to the phase/frequency detector, where it is compared with the 100 kHz reference signal. The error voltage output of the detector is integrated and becomes the tuning voltage for the VCXO. The phase locked loop has a bandwidth of approximately 30 Hz.

The 9 to 10 MHz signal output from the DDS goes to the DAC, where it is converted from a digitally encoded sine wave to a true analog sine wave. This signal goes through a 10 MHz low-pass-filter that filters out the 26.84 MHz clock frequency. It also fil-

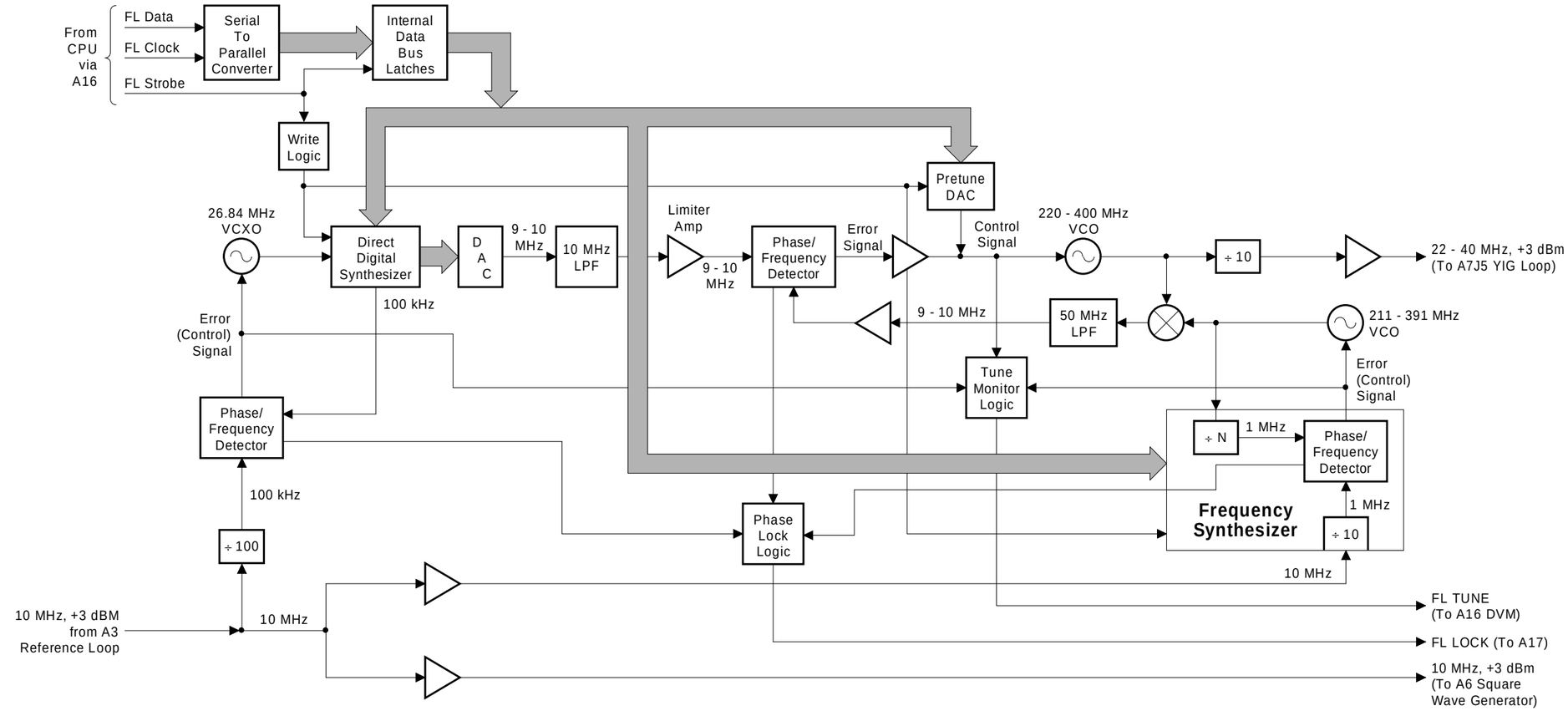


Figure 2-7. Block Diagram of the A5 Fine Loop PCB

ters out any mixing products of the clock frequency and the output frequency. The filtered 9 to 10 MHz signal is then fed to a limiter/amplifier. The limiting action of the amplifier reduces the level of the closely spaced AM spurs that cause an apparent degradation of the noise floor. The limiter/amplifier output is converted to TTL signal levels and becomes the 9 to 10 MHz reference frequency input to the fine loop phase/frequency detector.

Fine Loop Oscillator Pre-Tuning

The fine loop oscillator is tuned close to the correct output frequency by the pre-tune DAC. It is then phase locked by the fine loop phase-lock loop. The use of the pre-tune DAC speeds up the tuning of the oscillator which reduces lock acquisition time. It also lets the loop operate at close to 0 volts when locked, thus allowing maximum signal swing for improved acquisition. The pre-tune DAC receives its tuning information from the CPU via the serial interface.

Fine Loop Oscillator Phase Locking

The fine loop phase/frequency detector compares the 9 to 10 MHz IF signal, produced by the fine loop mixer, to the 9 to 10 MHz reference signal that is generated by the DDS. If there is a difference, the detector generates an error voltage. This loop error voltage adjusts the fine loop oscillator's output frequency to phase lock it to the 9 to 10 MHz reference.

Fine Loop Monitoring

Each loop on the A5 Fine Loop PCB generates a lock signal to indicate that it is phase locked. The three lock signals are fed to an AND gate that provides the status signal FL_LOCK to the CPU. The phase-error signal for each loop is fed to the tune monitor logic circuit. When directed by the CPU, the phase-error signal for the selected loop goes as FL_MON to the DVM circuit on the A16 PCB for use in calibration and troubleshooting.

Serial Interface

The CPU sends programming, tuning, and divider control data to the fine loop via the A16 PCB as 16-bit serial data words. The serial data is clocked into the serial-to-parallel converter by the fine loop clock signal. Upon completion of a 16-bit data transfer, the fine loop strobe signal loads the data into the internal parallel data bus latches. The strobe also triggers the logic circuits that write the data to the DDS, the pre-tune DAC, and the frequency synthesizer.

2-9 A6 SQUARE WAVE GENERATOR PCB

The A6 Square Wave Generator PCB (Figure 2-8) provides the internal square wave generating function for the sweep generator. It also supplies 400 kHz to phase lock the instrument's power supply.

Generating Square Waves

The square wave frequencies are derived from the 10 MHz reference frequency input using a combination of fixed and programmable dividers. The 10 MHz reference frequency input, received from the A5 Fine Loop PCB, is converted to TTL levels. It then goes to a ÷10 divider. The resultant 1 MHz signal is fed to the 12-bit programmable dividers. These dividers can be programmed to provide up to 4096 divider ratios. The divider values used to program the dividers are received from the CPU via the serial interface.

The signal output from the programmable dividers goes to a ÷2 divider. This divider returns the square wave signal to a 50% duty cycle. From this divider, the square wave signal goes via a line driver to pin 7 of the PCB connector. From here, the square wave signals are routed via the A20 Motherboard PCB to the A9 PIN Control PCB. There they are used to modulate the 681XXA's RF output.

NOTE

At the present time, the 681XXA firmware only supports generating four square wave frequencies—400 Hz, 1 kHz, 7.8125 kHz, and 27.8 kHz. These frequencies are selectable from a front panel menu.

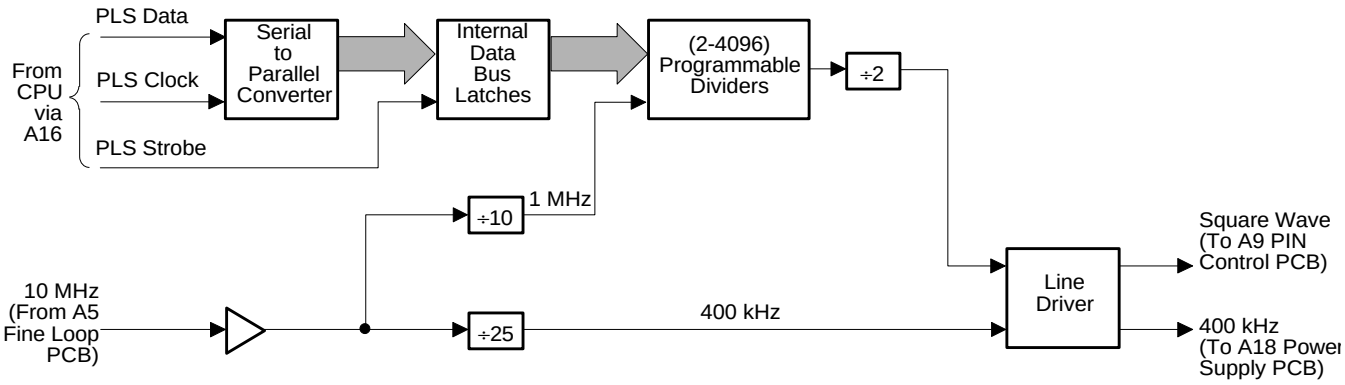


Figure 2-8. *Block Diagram of the A6 Square Wave Generator PCB*

Generating 400 kHz

The 10 MHz reference frequency input is fed to a ÷25 divider circuit to produce the 400 kHz signal. From the divider, the 400 kHz signal goes via a line driver to pin 15 of the PCB connector. From here, the signal is routed via the A20 Motherboard PCB to the A18 Power Supply PCB, where it is used to phase lock the power supply.

Serial Interface

The CPU sends divider control data to the square wave generator via the A16 PCB in a 16-bit serial data word format. The serial data word is clocked into the serial-to-parallel converter by the PLS clock signal. Upon completion of the 16-bit data word transfer, the PLS strobe signal loads the data into the internal parallel data bus latches.

2-10 A7 YIG LOOP PCB

The A7 YIG Loop PCB (Figure 2-9) provides for fine tuning and phase locking the YIG-tuned oscillator's output frequency to the reference frequency. This is accomplished by mixing a sample of the YIG-tuned oscillator's output frequency with harmonics of the coarse loop frequency. The resultant IF is then amplified and phase compared with the fine loop reference frequency.

The YIG Loop is divided into four functional groups—the power amplifier/divider, the step recovery diode/sampler, the IF amplifier/limiter, and the phase/frequency detector. These groups are mounted in individual housings designed to (1) maintain a high degree of isolation between the sensitive circuits of the YIG loop and (2) limit the amount of RF emissions within the instrument case that could be picked up by other sensitive circuits.

Power Amplifier/Divider The coarse loop output signal (439 to 490 MHz) is fed to the input of the power amplifier/divider circuit. The coarse loop frequency goes to a divider where it is divided by two to double the number of harmonics available. The divided frequency (219.5 to 245 MHz) is then amplified by the preamplifier/limiter and power amplifier to a level of +27 dBm. This level of power is required by the step recovery diode to generate harmonics of the coarse loop frequency.

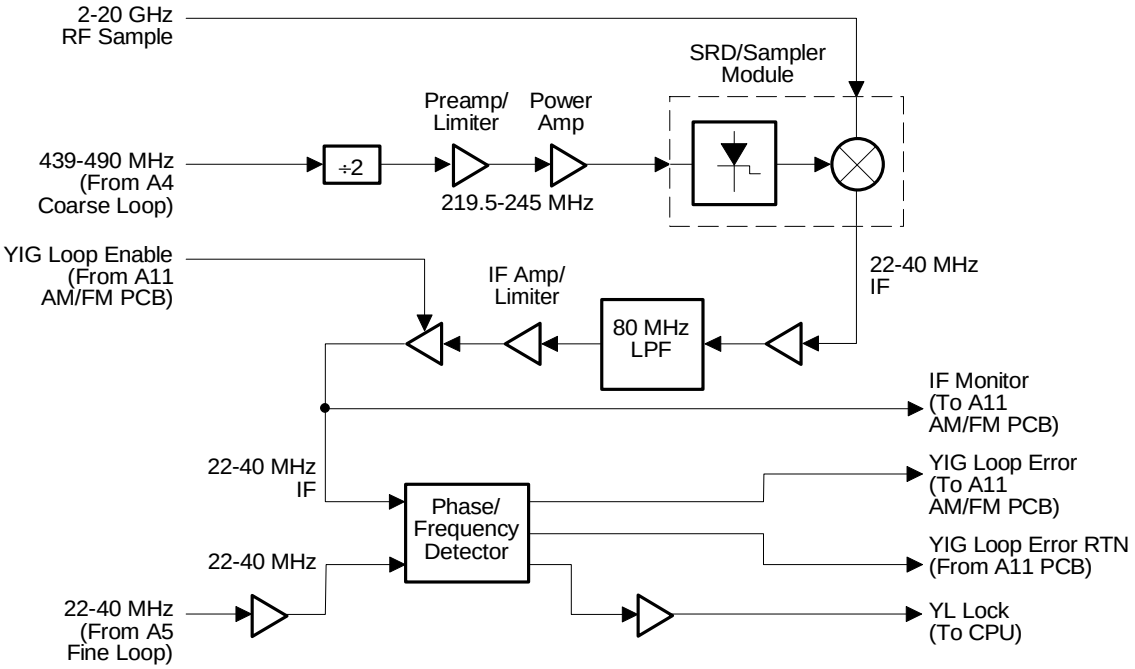


Figure 2-9. *Block Diagram of the A7 YIG Loop PCB*

Step Recovery Diode/ Sampler

The step recovery diode produces a very sharp impulse signal that contains harmonic signals in the range of ≥1.9755 to approximately 20 GHz. This harmonic comb output goes to the sampler, where it is mixed with a sample of the RF output from the YIG-tuned oscillator. The output of the sampler is an IF signal (22 to 40 MHz) that is fed to the IF amplifier/limiter.

IF Amplifier/ Limiter

The IF amplifier/limiter circuits amplify the IF signal from the sampler by a minimum of 40 dB. Limiting removes any residual AM information from the IF signal. An 80 MHz low-pass-filter is included in the IF amplifier to remove any undesirable products of the sampler mixing process. From the amplifier, the IF signal goes to the phase/frequency detector. The IF signal (IF MON) is also fed from the PCB to the DVM multiplexer circuit on the A11 PCB. When directed by the CPU, the IF signal is multiplexed from the A11 PCB to the DVM circuit on the A16 PCB for use in calibration and troubleshooting.

Phase Detector

The IF signal goes to the variable frequency input of the phase/frequency detector. The fine loop output frequency (22 to 40 MHz) is fed via an amplifier to the reference frequency input of the phase/frequency detector. The detector compares the two inputs and, if a difference exists, generates a loop error voltage. The loop error voltage is then sent to the A11 PCB. The A11 AM/FM PCB conditions the loop error voltage, producing a correction signal that is then fed to the A13 PCB. The A13 YIG Driver PCB uses this signal to fine tune and phase lock the YIG-tuned oscillator's output frequency to the reference frequency.

The A11 PCB provides a control signal (YIG Loop Enable) to disable the YIG loop during analog sweeps and unlocked FM mode of operation. This removes the IF signal from the input to the phase/frequency detector, thus preventing the detector from trying to follow the YIG-tuned oscillator's output frequency during fast analog sweeps. When the YIG loop is phase locked, the detector outputs a lock signal (YL Lock) to the CPU.

2-11 A9 PIN CONTROL PCB

The A9 PIN Control PCB (Figure 2-10 on page 2-39) provides current drive signals to the PIN switches located in the switched filter and frequency extension units, the drive signals for the optional step attenuator, and the modulator control for the ALC.

CPU Interface

The CPU controls the operation of the A9 PCB via the main processor bus (D0-D15). Whenever the PCB is addressed via L_SEL2, the data on the main processor bus is transferred by the data latches to the internal data bus (ID0-ID15). L_SEL2 also enables the address decoder, which decodes address lines A01-A03. The decoder circuit then strobes the addressed data latch(es) or DACs loading the instructions/data from the internal data bus.

Switched Filter PIN Drivers

The current drivers for the switched filter PIN switches are controlled by data loaded into an 8-bit data latch by strobe 2. The control data is then decoded by switch decoder circuits to turn on the appropriate PIN switch drivers. The decoders permit only certain current drivers to be turned on at the same time for protection of the circuitry inside the switched filter. This data latch also processes the data that controls the current driver for the notch filter PIN switch located in the YIG-tuned oscillator.

FEU PIN Drivers

The current drivers for the FEU PIN switches are used only for 681XXAs with a frequency range above 20 GHz. They are the same type drivers as those for the switched filter PIN switches and are also controlled by data loaded into an 8-bit data latch by strobe 2 and decoded by switch decoder circuits. The decoders allow only certain current drivers to be turned on at the same time to protect the FEU circuitry. There are also two spare PIN switch current drivers (for future use) that are controlled by this 8-bit data latch.

Step Attenuator/Relay Drivers

The drivers for the optional step attenuator are controlled by data loaded into an 8-bit data latch by strobe 0. The step attenuator may be a 3-section or 4-section attenuator. In addition, there are two relay drivers (for future use) that are controlled by this latch. Selection of dual DAC section A or B is also controlled via this data latch.

ALC Modulator Driver

The ALC modulator driver is a part of the ALC loop. It provides drive signals to the modulator, located in the switched filter, to adjust the RF output level.

The ALC modulator driver contains a shaper amplifier circuit, a FEU ALC amplifier circuit, a sample/hold circuit, and square wave modulation circuitry. It is controlled by data loaded into an 8-bit data latch by strobe 0.

Shaper Amplifier
The ALC control signal, from the A10 ALC PCB, is fed via a buffer/amplifier to the input of the shaper amplifier. (At frequencies above 20 GHz, the FEU ALC control signal, from the FEU ALC amplifier, is fed to the shaper amplifier's input.) The shaper amplifier circuit has a diode in the feedback path to increase circuit gain as the output goes above zero volts (approximately). This compensates for the decrease in the gain of the modulator due to the switched filter amplifiers going into compression.

Shaper amplifier gain is controlled by a control signal from the switched filter shaper DAC (section A of the dual DAC). The gain is adjusted so that the level amplifier on the A10 ALC PCB will have a more constant gain with power level changes. The shaper amplifier's output ranges from approximately +1 volt to approximately –3 volts. This modulator control voltage is fed via the square wave modulation driver to the switched filter modulator.

FEU ALC Amplifier
The FEU requires RF input power levels of +18 dBm in the 20 to 26.5 GHz range and +16 dBm in the 26.5 to 40 GHz range. The FEU ALC amplifier controls the RF input power level via the switched filter modulator and prevents overloading of the FEU doublers.

A portion of the 10 to 20 GHz RF input to the FEU is detected and fed to the A9 PCB. After amplification by the FEU detector preamplifier, the signal goes via the sample/hold circuit to the FEU ALC amplifier. Amplifier gain is controlled by a control signal from the FEU input level control DAC (section B of the dual DAC). From the FEU ALC amplifier, the level control output is routed to the input of the shaper amplifier.

The output of the FEU detector preamplifier (PIN MON) is also fed from the PCB to the DVM multiplexer on the A10 PCB. When directed by the CPU, the signal is multiplexed from the A10 PCB to the

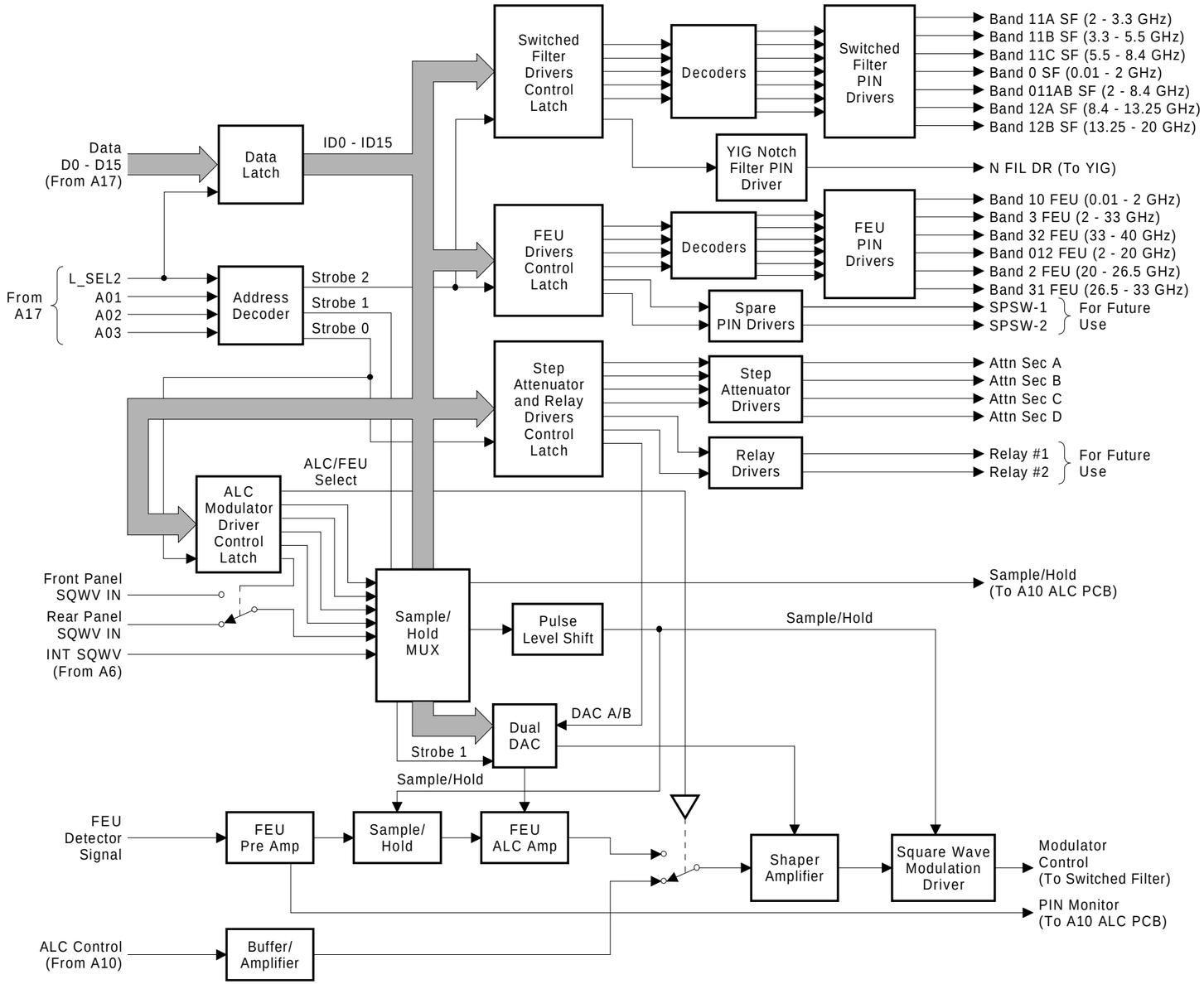


Figure 2-10. Block Diagram of the A9 PIN Control PCB

DVM circuit on the A16 PCB for use in calibration and troubleshooting.

Square Wave Modulation
The square wave modulation circuitry uses square wave inputs to modulate the RF output signal. There are two sources of square wave inputs.

- **INT SQWV**–Four TTL square wave frequencies (400 Hz, 1 kHz, 7.8125 kHz, and 27.8 kHz) that come from the A6 Square Wave Generator PCB. The frequencies are selectable from a front panel menu.
- **Front Panel SQWV IN and Rear Panel SQWV IN**–An external TTL square wave that comes from either the front panel or rear panel BNC input. The input is selectable from a front panel menu.

The square wave input signals are multiplexed by the sample/hold multiplexer. The multiplexer produces two sample/hold outputs. One output goes to the A10 ALC PCB, where it places the level amplifier in a HOLD mode during the periods the RF is turned off by the modulating square wave. This action prevents the ALC loop from changing the output level during these periods, which would cause distortion of the RF output waveform. This is necessary because the level amplifier cannot respond to the relatively fast rise times.

The other sample/hold output is fed to a pulse level shift circuit where the signal is shifted to a level necessary to drive the switching FETs of the square wave modulation driver and the sample/hold FETs of the FEU ALC amplifier.

During the ON portion of the modulating square wave, the normal ALC control voltage from the shaper amplifier is routed via the square wave modulation driver to the switched filter modulator. During the OFF portion of the modulating square wave, the ALC control voltage at the output of the shaper amplifier is in a HOLD mode because of the sample and hold input from the A10 ALC PCB. The square wave modulation driver then supplies approximately –3 volts to the switched filter modulator which causes it to go to its maximum attenuation state.

In the 20 to 40 GHz range, the sample/hold signal places the FEU ALC amplifier in a HOLD mode during the periods the RF is turned off by the modulating square wave.

2-12 A9-1 PIN CONTROL PCB

The A9-1 PIN Control PCB (Figure 2-11) provides current drive signals to the PIN switches in the switched filter and switched doubler module units, the drive signal for the optional step attenuator, and the modulator control for the ALC.

CPU Interface The CPU controls the operation of the A9 PCB via the main processor bus (D0-D15). Whenever the PCB is addressed via L_SEL2, the data on the main processor bus is transferred by the data latches to the internal data bus (ID0-ID15).

Programmable Logic Device The programmable logic device (PLD) controls all devices on the circuit board except for the dual DAC. The PLD is programmed to contain an address decoder, data latches, and a switch decoder. L_SEL2 enables the address decoder to decode address lines A01 and A02. The decoder circuit then strobes the addressed data latch or dual DAC and loads the instructions/data from the internal data bus.

Switched Filter PIN Drivers The current drivers for the switched filter PIN switches are controlled by data loaded into one of the PLD data latches. The control data is decoded by the PLD switch decoder. The decoder allows only certain current drivers to be turned on concurrently for protection of the switched filter circuitry. This PLD data latch also processes the data that controls the current driver for the notch filter PIN switch located in the YIG-tuned oscillator.

SDM PIN Drivers The current drivers for the SDM PIN switches are used only for 681XXA models with a frequency range above 20 GHz. The SDM PIN switch current drivers are controlled by data loaded into one of the PLD data latches and decoded by the PLD switch decoder. The decoder permits only one current driver to be turned on at a time for protection of the circuitry inside the SDM. There are also two spare PIN switch current drivers (for future use) that are controlled by this data latch.

Step Attenuator/Relay Drivers The drivers for the optional step attenuator are controlled by data loaded into a PLD data latch. The step attenuator may be a 3-section or 4-section attenuator. In addition, there are two relay drivers (for future use) that are controlled by this PLD data latch. Selection of dual DAC section A or B is also controlled via this data latch.

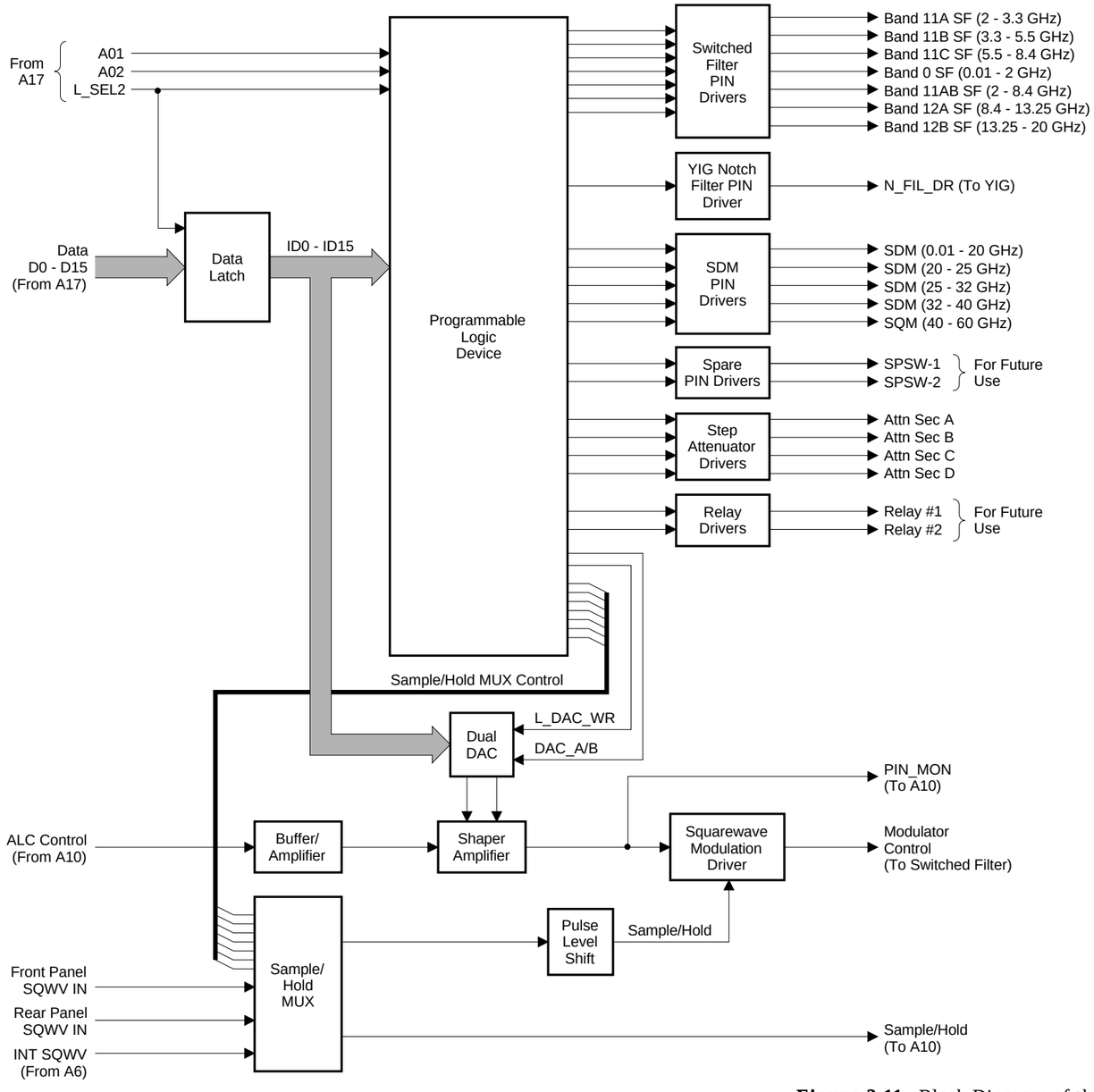


Figure 2-11. Block Diagram of the A9-1 PIN Control PCB

ALC Modulator Driver

The ALC modulator driver is a part of the ALC loop. It provides drive signals to the modulator, located in the switched filter, to adjust the RF output level. The ALC modulator driver contains a shaper amplifier circuit, a sample/hold circuit, and a square wave modulation circuit.

Shaper Amplifier

The ALC control signal, from the A10 ALC PCB, is fed via a buffer/amplifier to the input of the shaper amplifier. The shaper amplifier circuit has a diode in the feedback path to increase circuit gain as the output goes above zero volts (approximately). This compensates for the decrease in gain of the modulator due to switched filter amplifiers going into compression.

Shaper amplifier gain is controlled by a control signal from the switched filter shaper DAC (section A of the dual DAC). The gain is adjusted so that the level amplifier on the A10 ALC PCB will have a more constant gain with power level changes. The shaper amplifier's output ranges from approximately +1 volt to approximately –3 volts. The clamper DAC (section B of the dual DAC) controls the positive swing of the shaper amplifier's output to be from approximately +1 volt to approximately –1 volt. This prevents overdriving of either the high power switched filter amplifiers or the SDM amplifier.

The ALC control voltage output from the shaper amplifier is fed via the square wave modulation driver to the switched filter modulator. The output of the shaper amplifier (PIN MON) is also fed from the PCB to the DVM multiplexer on the A10 PCB. When directed by the CPU, the signal is multiplexed from the A10 PCB to the DVM circuit on the A16 PCB for use in calibration and troubleshooting.

Square Wave Modulation

The square wave modulation circuitry uses square wave inputs to modulate the RF output signal. There are two sources of square wave inputs.

- **INT SQWV**–Four TTL square wave frequencies (400 Hz, 1 kHz, 7.8125 kHz, and 27.8 kHz) that come from the A6 Square Wave Generator PCB. The frequencies are selectable from a front panel menu.

- **Front Panel SQWV IN and Rear Panel SQWV IN**–An external TTL square wave that comes from either the front panel or rear panel BNC input. The input is selectable from a front panel menu.

The square wave input signals are multiplexed by the sample/hold multiplexer, which is controlled by data loaded into a PLD data latch. The multiplexer produces two sample/hold outputs. One output goes to the A10 ALC PCB, where it places the level amplifier in a HOLD mode during the periods the RF is turned off by the modulating square wave. This action prevents the ALC loop from changing the output level during these periods, which would cause distortion of the RF output waveform. This is necessary because the level amplifier cannot respond to the relatively fast rise times.

The other sample/hold output is fed to a pulse level shift circuit, where the signal is shifted to a level necessary to drive the switching FETs of the square wave modulation driver.

During the ON portion of the modulating square wave, the normal ALC control voltage from the shaper amplifier is routed via the square wave modulation driver to the switched filter modulator. During the OFF portion, the ALC control voltage at the output of the shaper amplifier is in a HOLD mode because of the sample and hold input from the A10 ALC PCB. The square wave modulation driver then supplies approximately –3 volts to the switched filter modulator which causes it to go to its maximum attenuation state.

2-13 A10 ALC PCB

The A10 ALC PCB (Figure 2-12) controls the RF output power level functions of the 681XXA. It also provides amplitude modulation capability and control of the RF during square wave modulation. It is the major component of the automatic level control (ALC) loop (described on page 2-14).

CPU Interface

The CPU controls the operation of the A10 PCB via the main processor bus (D0-D15). Whenever the PCB is addressed via L_SEL3, the data on the main processor bus is transferred by the data latches to the ALC internal data bus (ID0-ID15). L_SEL3 also enables the ALC address decoder, which decodes address lines A01-A03. The decoder circuit then strobes the addressed ALC data latch(es) or DACs. This loads the instructions/data from the internal data bus to the addressed device. There are three data latches for controlling the functions of the ALC.

Level Reference Voltage

The Level Reference DAC provides the reference voltage for the ALC level amplifier. It is a 12-bit DAC that provides 0.01 dB resolution over a 40 dB level control range. Its reference voltage is supplied by part of the ALC Gain Calibration DAC. Adjusting the RF power level, using either the front panel keys or GPIB commands, causes the CPU to set the output voltage level from the Level Reference DAC equal to that of the desired RF output level.

ALC Slope

This circuit compensates for an increasing or decreasing output power-vs-frequency characteristic of the microwave components. The ALC Slope signal input to the A10 PCB is generated from the V/GHz signal on the A12 Analog Instruction PCB. The ALC Slope signal has a linear voltage change for a linear change in frequency. It is fed via a differential receiver to the Slope DAC.

The ALC Slope DAC is calibrated to compensate for the decreasing output power-vs-increasing frequency characteristics of the internal level detectors and optional step attenuator. It has a level control range of approximately ±10 dB. In addition, the operator can also adjust the Slope DAC's output to compensate for the output power-vs-frequency characteristics of external components connected to the RF output. This adjustment is made from a front panel menu. The voltage output of the Slope DAC is summed with the ALC reference voltage, the AM voltage, and the detector output voltage.

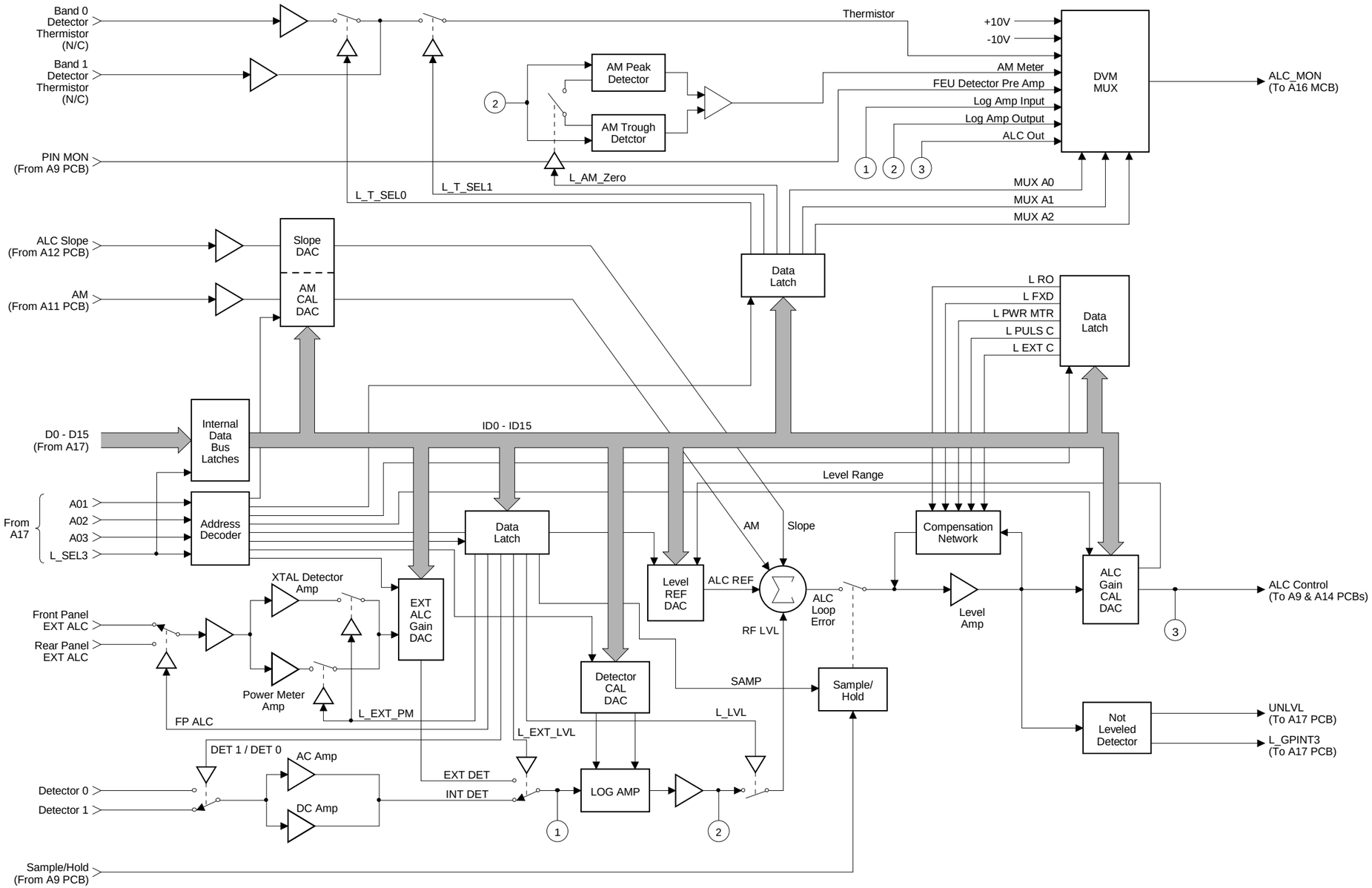


Figure 2-12. Block Diagram of the A10 ALC PCB

Amplitude Modulation

There are two AM operation modes—Linear AM and Log AM. In Linear AM mode, sensitivity is 100%/V and the 681XXA accepts a –1V to +1V input signal. In Log AM mode, sensitivity is 10 dB/V and the signal generator accepts a wider range of input signals. Selection of the AM operation mode is made from a front panel menu or via GPIB command.

The external AM input to the 681XXA first goes to the A11 AM/FM PCB where it is conditioned according to the operating mode selected. It then goes to the AM input of the A10 PCB. The AM input is fed via a differential receiver to the AM Calibration DAC. The AM Calibration DAC is calibrated to adjust its output for the proper amount of AM in both the Linear AM and Log AM operating modes. The voltage output of the AM Calibration DAC is summed with the ALC reference voltage, the ALC slope voltage, and the detector output voltage.

External ALC

In the external leveling mode, an output from an external crystal detector or power meter is used as the feedback input to the ALC loop. The signal's polarity may be either positive or negative. The external ALC signal may be connected to either the front panel or rear panel EXT ALC IN connector.

The external ALC signal, from the front or rear panel, is connected through relay contacts to a preamplifier/buffer. The relay is controlled from a front panel menu. The buffered ALC signal goes to two amplifiers—the crystal detector amplifier and the power meter amplifier. For detector leveling, the output of the crystal detector amplifier is fed to the External ALC Gain DAC. For power meter leveling, the output of the power meter amplifier is fed to the External ALC Gain DAC. Amplifier output selection is controlled from a front panel menu.

The External ALC Gain DAC permits calibration for various sensitivities of crystal detectors and power meters. It is adjusted from the front panel for proper gain. The output of the External ALC Gain DAC goes to the input of the detector log amplifier.

Internal ALC

In the internal leveling mode, a signal from an internal level detector is used as a feedback input to the ALC loop. There are two internal level detectors–Detector 0 and Detector 1. Detector 0 is part of the Down Converter and is for frequencies from 0.01 to

2 GHz; Detector 1 is part of the main Directional Coupler and is for frequencies from 2 to 40 GHz. These detector signals are multiplexed by FET switches into the detector preamplifier. The preamplifier contains separate amplifiers for the AC and DC portions of the detector signal. The output of the detector preamplifier goes to the input of the detector log amplifier.

Detector Log Amplifier

The internal and external detector signals, from the detector preamplifier and the External ALC Gain DAC respectively, are multiplexed by a relay to the input of the detector log amplifier circuit. The detector log amplifier compresses the detector signal to produce a volts-per-dB characteristic at the log amplifier output. The Detector Calibration DAC adjusts log shaping to compensate for variations in square-law to linear transition for different detectors, and nulls preamplifier offset voltage. The output of the log amplifier is fed via a switch to the input of the level amplifier. There it is summed with the ALC reference voltage, the ALC slope voltage, and the AM voltage. During the fixed gain mode of operation, the switch is open to interrupt the ALC loop.

ALC Loop Error Signal

When the RF output of the 681XXA is leveled, the sum of the ALC reference voltage, the ALC slope voltage, and the AM voltage should be equal to the detector log amplifier voltage. But its polarity should be opposite. The result of summing these voltages is a loop error voltage of zero.

Whenever the RF output becomes unleveled, summing these voltages will result in an ALC loop error voltage. This error signal is used to adjust the RF output to obtain the requested output level. The ALC loop error signal is fed via the sample/hold FET switches to the level amplifier.

Sample/Hold Circuit

Normally, the ALC loop error signal passes unimpeded through the sample/hold FET switches to the input of the level amplifier. During square wave modulation, however, the sample/hold FET switches are switched on and off in sync with the modulating signal. This causes the level amplifier to operate as a sample/hold amplifier. The sample/hold circuit is activated by the sample/hold signal from the A9 Pin Control PCB.

During the ON portion of the modulating square wave, the ALC loop error signal is fed to the level amplifier to control the RF output level. During the OFF portion of the modulating square wave, the FET switch opens. This interrupts the signal path and places the level amplifier in a HOLD mode. Because the ALC is only active when RF is present, it does not need to follow the very rapid pulse transitions (which would cause distortion of the RF output waveform).

Level Amplifier

The level amplifier amplifies the ALC loop error signal so that a large amount of level corrections can be achieved with negligible error. A compensation network in the feedback path of the level amplifier is used to change the bandwidth of the ALC loop during different modes of operation. The output of the level amplifier is fed to the ALC Gain Calibration DAC and the Not Leveled Detector.

ALC Gain Cal DAC

The ALC Gain Calibration DAC allows adjustment of the overall ALC loop gain to compensate for the gain variations of the modulators and crystal detectors. The DAC is calibrated for each individual frequency band. This provides a more consistent loop gain and loop bandwidth throughout the frequency range. The output of the ALC Gain Calibration DAC is the ALC control signal, which has a sensitivity of approximately 10 dB/V. The ALC control signal goes to the modulator driver on the A9 PIN Control PCB. For models containing the Frequency Extension Unit, the ALC control signal also goes to the modulator driver on the A14 Doubler Driver PCB.

Not Leveled Detector

The not leveled detector is a window comparator that monitors the output signal from the level amplifier. If the RF output is too high or does not reach the power level selected, the level amplifier's output signal goes outside its normal operating range. When this occurs, the detector sends an interrupt signal, L_GPINT3, to the CPU. The CPU will then write the message, UNLEVELED, on the front panel LCD. The CPU monitors the not leveled detector via the UNLVL status line and will continue to display the warning message while the not leveled condition exists.

Detector Thermistor Circuit

In the 681XXA, the CPU does *not* monitor the output of the thermistor that is built into each internal level detector. The thermistor signal is not connected to the A10 PCB and the thermistor circuitry on the A10 PCB is disabled by the control signals, L_T_SEL0 and L_T_SEL1, from the ALC data latch.

AM Meter Circuit

The AM meter circuit consists of an AM peak detector and an AM trough detector. The detectors rectify the output signal from the detector log amplifier. Summing the resulting positive and negative peak-detected voltages together produces a dc output voltage that is approximately 200 mV/dB peak-to-peak. The output voltage is routed via the DVM multiplexer to the DVM circuit on the A16 PCB. The DVM circuit converts the voltage to a %AM. During AM measurements, the zeroing of the AM meter circuit by the zero switch occurs at approximately a 100 mS interval. This allows for faster indications of AM changes.

DVM Multiplexer

The DVM multiplexer is used for multiplexing various signals from the A10 PCB to the DVM circuit on the A16 PCB. The following signals are multiplexed to the DVM for self test, measurement, and/or calibration purposes:

- +10V and –10V reference voltages
- Detector Log Amplifier input
- Detector Log Amplifier output
- FEU detector preamplifier output (from the A9 PCB)
- ALC Control output
- AM Meter circuit output

2-14 A11 AM/FM PCB

The A11 AM/FM PCB (Figure 2-13) provides the capability for phase locking, frequency modulating (FM), and narrow-band analog sweeping (≤100 Hz wide) of the YIG-tuned oscillator RF output. In addition, the A11 PCB contains the input circuitry for the amplitude modulating signal that goes to the A10 ALC PCB.

CPU Interface

The CPU controls all of the functions of the A11 PCB via the main processor bus (D0-D15). Whenever the PCB is addressed via L_SEL4, the data on the main processor bus is transferred by the data latches to the internal data bus (ID0-ID15). L_SEL4 also enables the address decoder, which decodes address lines A01-A03. The decoder circuit then strobes the addressed data latch(es) or DACs loading the instructions/data from the internal data bus. There are two data latches that control the FM driver functions and one data latch that controls the DVM multiplexer and AM input circuits.

FM Input Circuitry

The external FM signal input comes from either the front panel or rear panel FM IN connectors (selectable from a front panel menu). The external FM signal goes (via the overload detector and the contacts of the internal/external FM path switch) to the buffer amplifier. The normal external input impedance is 600 ohms; however, 50 ohms may be selected by the operator from the front panel menu.

Whenever the overload detector encounters an external FM signal over 5 volts peak, it switches to the internal FM path and sends the status signal FM_OVLD to the CPU. The CPU then writes the messages, **ERR** and **Reduce FM Input Level**, on the front panel LCD. The CPU monitors the FM overload status line and displays the messages continuously while the overload condition exists.

From the unity gain buffer amplifier, the FM signal goes to a filter network. The filter network consists of three signal paths. The FM mode of operation determines which path is selected for use. The DC path is used in the unlocked FM mode of operation; the paths containing the 1 kHz HPF (for FM deviations of >300 kHz/V) and 30 Hz HPF (for FM deviations of ≤300 kHz/V) are used in the phase-locked FM mode of operation. *In the 681XXA, only the DC path is used.* This is because the YIG phase-lock loop is always disabled during FM mode to achieve greater FM deviations.

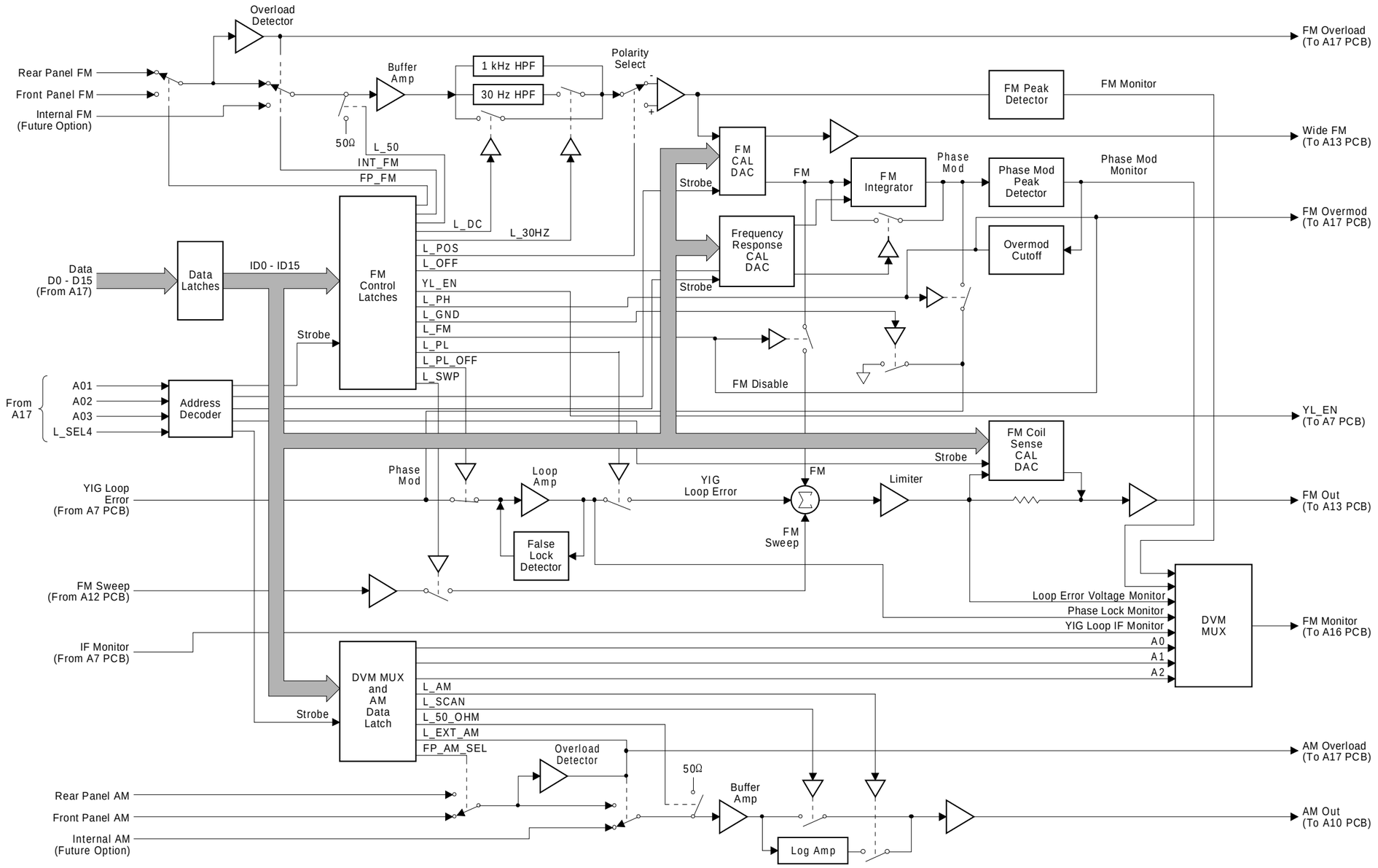


Figure 2-13. Block Diagram of the A11 AM/FM PCB

From the filter network, the FM signal goes via a polarity select switch to a buffer amplifier. FM signal polarity is selectable from a front panel menu. The FM signal from the buffer amplifier is fed to the FM Calibration DAC and the FM Meter circuit.

FM Meter Circuit

The FM meter circuit is a full-wave rectifier that produces a voltage proportional to the peak input FM signal. This voltage is routed via the DVM multiplexer to the DVM circuit on the A16 PCB.

FM Calibration DAC

The FM Calibration DAC is used to calibrate the input sensitivities of the FM circuit. The input sensitivities (–6 MHz/V, +10 MHz/V, and +20 MHz/V) are selectable from a front panel menu.

There are two FM modes of operation–wide and narrow. When the wide FM mode is selected, the FM signal is fed from the FM Calibration DAC via a buffer amplifier to the A13 YIG Driver PCB. In this mode, the normal FM paths on the circuit board are open. On the A13 PCB, the FM signal is applied to the main tuning coil driver of the YIG-tuned oscillator. This allows maximum FM deviations of 100 MHz.

When the narrow FM mode is selected, the FM signal is fed from the FM Calibration DAC via an analog switch to the Limiter.

Phase-Locked FM

The 681XXA does *not* have a FM phase-locked mode of operation. During FM modes, the control signal, YL_EN, is sent to the A7 YIG Loop PCB to disable the YIG loop. As a consequence, the FM Integrator, Frequency Response Calibration DAC, Phase Modulation Peak Detector, and Overmodulation Cutoff circuits are not used and are disabled by control signals from the FM control latches.

FM Sweep

During narrow-band analog sweeps (≤100 MHz wide), the sweep ramp signal from the A12 Analog Instruction PCB is fed via a buffer amplifier and an analog switch to the Limiter. The control signal, YL_EN, is sent to the A7 YIG Loop PCB during analog sweeps to disable the YIG loop.

YIG Phase-Lock

During YIG loop phase locking, the loop error voltage from the A7 YIG Loop PCB goes to the loop amplifier. The loop amplifier has a decreasing gain with increasing frequency characteristic. The false lock detector prevents the loop from phase locking on noise by generating a voltage that forces the YIG-tuned oscillator to a higher frequency when a false lock is detected. From the loop amplifier, the loop error voltage is fed via an analog switch to the Limiter. Whenever the YIG loop is unlocked (in analog sweep mode or FM mode), the switch is opened. This disconnects the output of the loop amplifier and prevents the YIG FM coil from receiving an erroneous phase-error voltage.

The loop error voltage at the loop amplifier output is connected via the DVM mutliplexer to the DVM circuit on the A16 PCB. Once phase-lock is acquired, this voltage is monitored and adjusted to zero by the Center Frequency DAC on the A12 PCB.

Limiter

The limiter circuit prevents the YIG FM coil from being overdriven. It limits the maximum FM modulation deviation to approximately 50 MHz. There are three inputs to the limiter circuit:

- The YIG loop error voltage from the loop amplifier during YIG loop phase-locking.
- The FM signal from the FM Sensitivity DAC during narrow FM mode of operation.
- The sweep ramp signal from the A12 Analog Instruction PCB during narrow-band analog sweeps (≤100 MHz wide).

FM Coil Sensitivity Circuit

The FM Coil Sensitivity Calibration DAC is used to calibrate the FM modulation sensitivity of the YIG-tuned oscillator's FM coil. This is to compensate for the slight variation in sensitivity of each band of the YIG-tuned oscillator. The output of the Limiter goes to the input of the FM Coil Sensitivity Calibration DAC. The outputs of the Limiter and the DAC are then combined by the buffer amplifier to produce an FM output signal that has a 10 MHz/V sensitivity. The FM output signal goes to the A13 YIG Driver PCB.

DVM Multiplexer

The DVM multiplexer is used for multiplexing various signals from the A11 PCB to the DVM circuit on the A16 PCB. The following signals are multiplexed to the DVM for self-test, measurement, and/or calibration purposes:

- FM Meter circuit output
- Phase Modulation Meter circuit output
- IF Amplifier output (from the A7 PCB)
- Loop Amplifier output
- Limiter output

AM Input Circuitry

The external AM signal input comes from either the front panel or rear panel AM IN connector (selectable from a front panel menu). The external AM signal goes to the buffer amplifier via an overload detector and the contacts of the internal/external FM path switch. The normal external input impedance is 600 ohms, however, 50 ohms may be selected by the operator from the front panel menu.

Whenever the overload detector encounters an external AM signal over 5 volts peak, it switches to the internal AM path and sends the status signal, AM_OVLD to the CPU. The CPU then writes the messages, **ERR** and **Reduce AM Input Level**, on the front panel LCD. The CPU monitors the AM overload status line and displays the messages continuously while the overload condition exists.

From the buffer amplifier, routing of the AM signal is determined by the AM mode of operation selected. There are two AM operation modes—Linear AM and Log AM. When the Linear AM mode is selected, the AM signal goes to the logarithmic amplifier. Because the leveling loop is logarithmic, the AM signal must be logarithmic to obtain true linear AM modulation. (The amplitude of the RF output changes linearly as the modulating voltage changes.) From the logarithmic amplifier, the AM signal goes via a buffer amplifier to the A10 PCB.

When the Log AM mode is selected, the AM signal bypasses the logarithmic amplifier and goes directly to the buffer amplifier for output to the A10 PCB. In logarithmic AM modulation, the amplitude of the RF output changes in dB with a linear change in modulating voltage.

2-15 A12 ANALOG INSTRUCTION PCB

The A12 Analog Instruction PCB (Figure 2-14 on page 2-59) provides frequency tuning voltages and frequency band select signals to the A13 YIG Driver PCB. For models with a frequency range greater than 20 GHz, it supplies frequency band select signals to the A14 Doubler Driver PCB or A14-1 SDM Driver PCB. In addition, it provides HORIZ OUT and V/GHz OUT signals to the rear panel of the sweep generator. It also provides a SLOPE signal to the A10 ALC PCB for slope-vs-frequency correction of the RF output power.

CPU Interface

The CPU controls the operation of the A12 PCB via the main processor bus (D0-D15). Whenever the PCB is addressed via L_SEL5, the data on the main processor bus is transferred by the data latches to the internal data bus (ID0-ID15). L_SEL5 also enables the address decoder, which decodes address lines A01-A04. The decoder circuit then strobes the addressed data latch(es) or DACs loading the instructions/data from the internal data bus. There are two data latches that control the ramp generator circuits and the DVM multiplexer, and two data latches that supply frequency band select signals.

Frequency Band Selection

Frequency band selection signals are sent by the CPU via the two data latches to the A13 YIG Driver PCB and the A14 Doubler Driver or A14-1 SDM Driver PCBs. These signals control the bias voltages for the YIG oscillator and amplifiers in the switched filter, the down converter, and the FEU or SDM.

These data latches also provide three signals (L_BAND1, CW_FILT_1, and L_LFM) that control the operation of the A13 YIG Driver PCB as follows:

- L_BAND1 enables the FM signal from the A11 PCB and the Tune signal from the A12 PCB.
- CW_FILT_1 enables the CW filter for the main coil of the YIG-tuned oscillator for CW operation and narrow band analog sweeps.
- L_LFM enables the Wide FM signal from the A11 PCB.

±10V Reference Supplies

The ±10V reference supplies furnish the reference voltages for the DACs on the Analog Instruction PCB. They are also used for calibrating the DVM located on the A16 CPU Interface PCB.

Ramp Generator Circuitry

The ramp generator circuitry provides a linear analog sweep ramp with a dwell at the top and bottom of the ramp to allow for bandswitching and phase-locking of the oscillators for frequency correction. In addition, it establishes bandswitch points for broadband sweeps and frequency marker placement. It consists of the Sweep Time DAC, the Ramp Integrator, the Ramp Comparator, the Marker Switch Point DAC, the Ramp Control Logic, and the Ramp Calibration DAC.

Ramp Integrator

During forward sweeps, the Sweep Time DAC supplies a current to charge the ramp integrator capacitor. There are three charging paths—one for sweep times of ≤1 second, one for sweep times of >1 second, and one for ramp retrace. The signal, L_T<1SEC, closes the analog switch selecting the ≤1 second charging path. During sweep retrace, ramp control logic signals disconnect the Sweep Time DAC and connect the charging path to –10V. During CW modes of operation, the signal, L_INT_OFF, closes the analog switch that disables the ramp integrator.

The ramp integrator output is a linear ramp signal. The top (high end) of the ramp is –10 volts and the bottom (low end) of the ramp is 0 volts. The ramp signal goes via the contacts of relay K1 to (1) a buffer amplifier for input to the frequency instruction circuits, (2) a buffer amplifier for input to the horizontal output and V/GHz circuits, and (3) the ramp comparator.

Ramp Comparator and Marker Switch Point DAC

One input to the ramp comparator is the ramp signal from the ramp integrator; the other input is the output from the Marker Switch Point DAC. The DAC is set for a voltage that corresponds to the frequency where a bandswitch or marker must occur. For the top of the sweep, it is set for a –10 volts; for the bottom of the sweep, it is set for 0 volts.

When the ramp reaches a voltage that corresponds to a bandswitch point, a marker, or the top or bottom of the ramp, the ramp comparator generates a logic signal to the ramp control logic that starts the dwell.

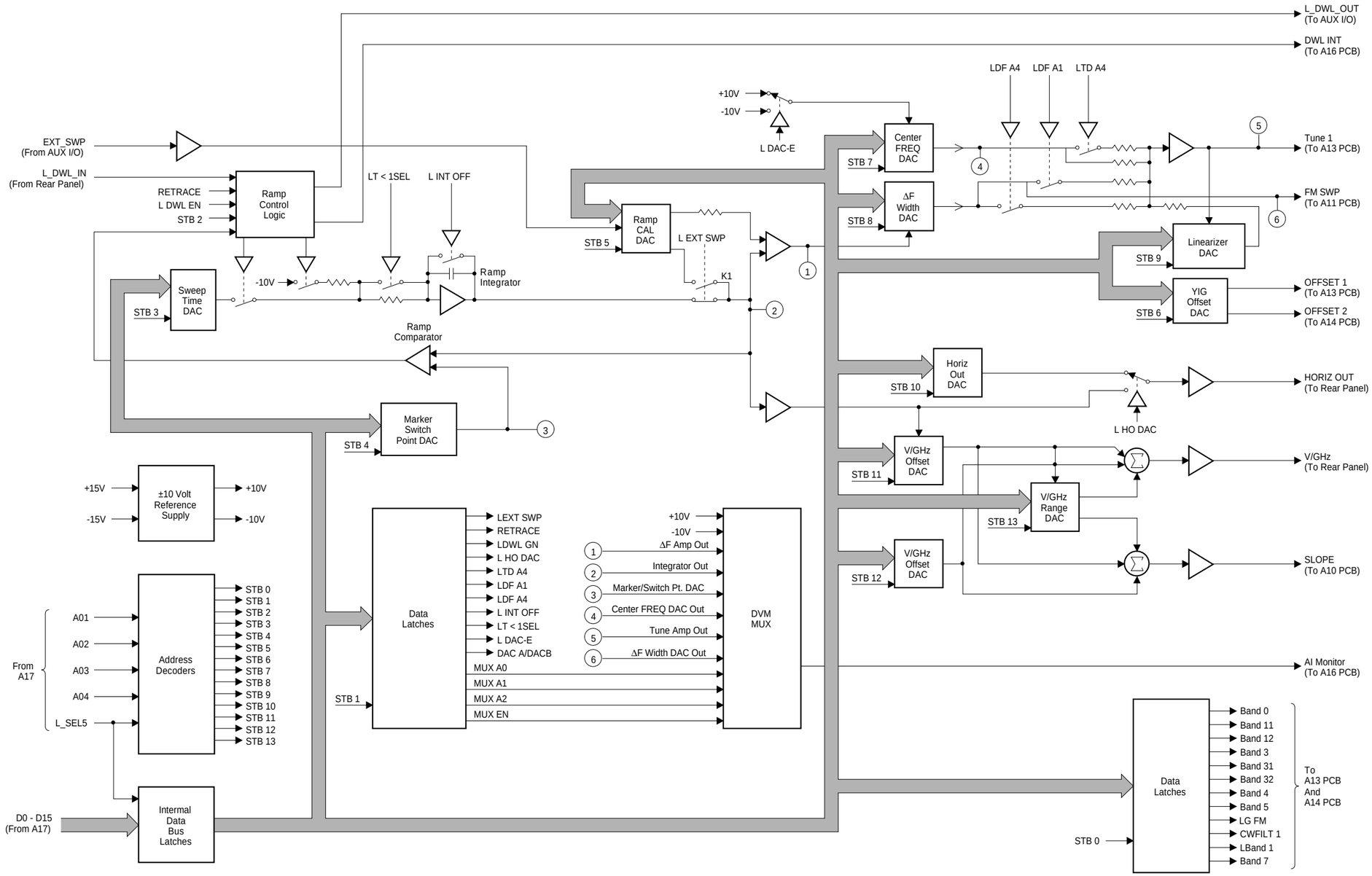


Figure 2-14. Block Diagram of the A12 Analog Instruction PCB

Ramp Control Logic
Ramp control logic determines when the ramp is in the sweep, retrace, or dwell mode. The dwell signal from the ramp comparator (or L_DWL_IN from the rear panel) determines the start of each dwell. All other control signals and timing are determined by the CPU. L_DWL_EN enables the dwell signal from the ramp comparator, STB2 terminates the dwell, and RETRACE determines if the ramp is sweeping or retracing.

When the ramp comparator sends a dwell signal, the ramp control logic stops the analog sweep by opening the switch that applies the charging current from the Sweep Time DAC. It also sends the interrupt signal, DWL_INT, to the CPU via the A16 PCB. Upon receiving the dwell interrupt, the CPU takes over control of the ramp and sets L_DWL_EN false (high) for the duration of the dwell. After completing its tasks, the CPU sets L_DWL_EN true (low) and sends STB2 to terminate the dwell. The ramp will then resume in a positive or negative direction, depending on the condition of the RETRACE signal.

Whenever the rear panel signal, L_DWL_IN, goes true (low), the ramp control logic stops the analog sweep but does not generate the interrupt signal DWL_INT. When L_DWL_IN goes high again, the ramp will continue.

Ramp Calibration DAC
The 0 to –10V ramp signal from the ramp integrator goes via the contacts of K1 to a buffer amplifier before going to the ΔF Width DAC. The buffer amplifier doubles the ramp signal and applies a 10 volt offset to produce a –10V to +10V ΔF ramp signal. The Ramp Calibration DAC provides the 10 volt offset and it is used to calibrate the ΔF ramp for an equal + and – 10 volt swing.

Relay K1 provides for using an external ramp signal to replace that generated by the internal ramp generator. This provision is used to slave one 681XXA to another at a fixed offset frequency. The Ramp Calibration DAC is used to calibrate the Analog Instruction PCB to the external ramp. The L_DWL_OUT signal that is generated by the ramp control logic in response to a ramp comparator

dwell signal is also used for this master-slave operation of two 681XXAs.

Frequency Instruction Circuitry

The frequency instruction circuitry provides the analog tuning voltages to the A13 YIG Driver PCB in both CW and sweep modes of operation. The frequency instruction circuitry consists of the Center Frequency DAC, the ΔF Width DAC, and the Linearizer DAC.

Center Frequency DAC

The Center Frequency DAC supplies the tuning voltages for the A13 YIG Driver PCB in the CW or step sweep mode of operation and an offset voltage during analog sweep operation. It has two available output ranges, 0V to +10V and 0V to –10V, which are determined by the polarity of the 10V reference voltage applied to the DAC.

During CW and step sweep mode, the Center Frequency DAC generates a 0V to approximately +10V output. This voltage then goes via the unity gain path to the summing amplifier where it is inverted. The 0V to approximately –10V signal output from the summing amplifier goes to the A13 YIG Driver PCB to tune the YIG-tuned oscillator throughout its frequency range.

In analog sweep operations, the voltage outputs of the Center Frequency DAC and the ΔF Width DAC output are summed together to provide the 0V to –10V tuning signal to the A13 PCB for sweeps widths of >100 MHz. For sweep widths of ≤100 MHz, the voltage from the Center Frequency DAC is used to tune the YIG-tuned oscillator to a center frequency and the ramp voltage from the ΔF Width DAC is used to sweep the FM coil.

During broadband analog sweeps, the polarity of the Center Frequency DAC output is changed as necessary to provide a 0V to –10V tuning signal to the A13 PCB. To offset the very high ΔF ramp voltages encountered in broadband sweeps, the Center Frequency DAC output is fed via a gain-of-four path to the summing amplifier.

The settings of the Center Frequency DAC for each YIG-tuned oscillator are stored at the time of frequency calibration.

ΔF Width DAC
The ΔF Width DAC receives a +10V to –10V ΔF ramp from the ramp generator and attenuates it according to the selected sweep width. When sweeping a single YIG-tuned oscillator band, such as 2–8.4 GHz, the output of the ΔF Width DAC will go from approximately –5V to +5V. The Center Frequency DAC then sums a –5V offset with the attenuated ΔF ramp to provide the necessary 0V to –10V tuning range for the YIG-tuned oscillator. For sweeps of one oscillator band, the ΔF Width DAC output goes via a unity gain path to the summing amplifier.

When broadband sweeps are selected, such as 0.01–40 GHz, the ΔF ramp voltage from the ΔF Width DAC may go from –10V to +10V, depending on which frequency band is active. The output goes via a gain-of-four path to the summing amplifier to provide sufficient ΔF ramp slope to cover the frequency range of the YIG-tuned oscillators used.

In narrow band sweep widths (≤100 MHz), the ΔF ramp voltage from the ΔF Width DAC will go from approximately –9V to +10V. The ramp voltage, FM_SWP, goes to the A11 AM/FM PCB to sweep the FM coil of the YIG-tuned oscillator.

Linearizer DAC
YIG-tuned oscillators have a typical linearity of 0.01%. At higher frequencies, this can lead to a significant error (approximately 20 MHz @ 20 GHz). The Linearizer DAC reduces this non-linearity by approximately a five-to-one ratio.

The frequency instruction tuning output to the A13 YIG Driver PCB is also applied to the Linearizer DAC circuit. The output of this circuit, which is used to reduce linearity errors, is fed back to the input of the summing amplifier as either a positive or negative voltage. Both the breakpoint and the magnitude or slope of this feedback voltage are programmable. The settings of the Linearizer DAC are stored for each frequency band at the time of frequency calibration.

YIG Offset DAC

YIG Offset DAC A supplies a reference voltage (OFFSET_1) for the A13 YIG Driver PCB to set the low end operating frequency of the YIG-tuned oscillators. It provides coarse calibration of the start frequency of the oscillators while the Center Frequency DAC provides fine calibration of the start frequencies. The YIG Offset DAC A settings for each YIG-tuned oscillator are stored at the time of frequency calibration.

YIG Offset DAC B supplies a reference voltage (OFFSET_2) for the A14 Doubler Driver PCB to fine tune the modulator shaper amplifier gain for each FEU modulator. The YIG Offset DAC B settings for each FEU modulator are stored during calibration of the ALC for frequencies above 20 GHz.

Horizontal Output

During analog sweep and CW/with CW Ramp enabled modes, the ramp voltage from the ramp generator goes to a buffer amplifier that inverts it. The 0V to +10V ramp is then fed (1) to the V/GHz Width DAC and (2) via the closed contacts of an analog switch and a buffer amplifier to the A21 Rear Panel PCB as the signal HORIZ_OUT. When an external ramp signal is applied (during master-slave operation of two 681XXAs), it is also routed to the A21 Rear Panel PCB in the same manner as the internally generated ramp signal.

During CW or step sweep modes, the Horizontal Output DAC supplies the 0V to +10V ramp signal to the Rear Panel PCB via the analog switch contacts and the buffer amplifier. The signal, L_HO_DAC, controls the analog switch.

V/GHz Circuitry

The V/GHz circuitry consists of the V/GHz Width DAC, the V/GHz Offset DAC, the V/GHz Range DAC, and an output summing amplifier.

During analog sweep, the V/GHz Width DAC receives the buffered ramp signal from the ramp generator. It attenuates the ramp according to the sweep width and applies the attenuated ramp to the summing amplifier. Here, the ramp sums with an offset voltage provided by the V/GHz Offset DAC. In addition, the outputs of these two DACs are inverted and fed to the V/GHz Range DAC A. The output of the V/GHz Range DAC A goes to the summing amplifier. The summing amplifier, which has a gain of two, sums the outputs from the three

DACs to provide the V/GHz signal to the A21 Rear Panel PCB. For instruments with a high end frequency of 20 GHz or less, the output of the summing amplifier is 1.0 volt per GHz; for instruments having a high end frequency of 20–40 GHz, the output of the summing amplifier is 0.5 volt per GHz.

During CW or step sweep mode, the V/GHz Width DAC is set for minimum output and the outputs from the V/GHz Offset DAC and V/GHz Range DAC A are summed by the summing amplifier to produce the V/GHz signal.

Slope Circuitry

V/GHz Range DAC B provides an offset that sums with the outputs of the V/GHz Width DAC and the V/GHz Offset DAC at the summing amplifier so that at 2 GHz, the output of the summing amplifier is 0 volts. For instruments with a down converter, this allows independent control of the slope for below 2 GHz and for 2 GHz and above. The summing amplifier output signal, SLOPE, goes to the A10 ALC PCB where it is used by the ALC Slope DAC to compensate for any decreasing output power-vs-increasing frequency characteristics of the internal level detectors and optional step attenuators.

DVM Multiplexer

The DVM Multiplexer is used for multiplexing various signals from the A12 PCB to the DVM circuit on the A16 PCB. The following signals are multiplexed to the DVM for self test, measurement, and/or calibration purposes:

- +10V and –10V reference voltages
- ΔF Ramp Amplifier output
- Ramp Integrator output
- Marker Switch Point DAC output
- Center Frequency DAC output
- Summing Amplifier TUNE output
- ΔF Width DAC output

2-16 A13 YIG DRIVER PCB

The A13 YIG Driver PCB (Figure 2-15 on page 2-67) provides the tuning current and bias voltages for the 2 to 20 GHz YIG-tuned oscillator. It also supplies the bias voltages for the 0.01 to 2 GHz Down Converter and the amplifiers located in the Switched Filter.

FM Tuning Coil Driver

The FM signal output from the A11 AM/FM Driver PCB is routed to the input of a differential receiver. This signal is used for phase-locking the YIG loop, frequency modulation, and narrow-band analog sweeps (≤100 MHz wide). From the differential receiver, the FM signal goes via an analog switch to the input of the FM control amplifier. The analog switch is controlled by the signal, L_BAND_1, from the A12 Analog Instruction PCB.

The FM control amplifier and coil drivers convert the FM control voltage to FM tuning coil current. The FM tuning coil current sense resistor senses the output current through the FM coil and generates a feedback signal. The feedback signal is fed to the input of the FM control amplifier where it sums with the FM signal.

In CW and narrow-band (≤100 MHz wide) analog sweep modes, the signal, CW_FIL_1, closes an analog switch placing the CW filter network across the main tuning coil and connecting the FM tuning coil feedback signal to the control amplifier for the main tuning coil driver. Whenever the narrow-band sweep ramp is applied to the FM tuning coil, the FM tuning coil couples a small change in current to the main tuning coil causing a non-linear sweep. The feedback signal from the FM tuning coil is fed to the control amplifier for the main tuning coil driver to cancel the change in current in the main tuning coil. This produces a linear sweep for sweep widths of 100 MHz or less.

Main Tuning Coil Driver

There are three input signals to the control amplifier for the main tuning coil driver—OFFSET_1, TUNE_1, and LF_FM.

- OFFSET_1, from the A12 Analog Instruction PCB, is a reference voltage that sets the low end tuning current for the YIG-tuned oscillator. It is fed to the control amplifier via a buffer amplifier.

- TUNE_1, also from the A12 PCB, is a dc voltage that represents the tuning current needed for the YIG-tuned oscillator (CW mode) or a 0V to –10V ramp signal (sweep mode). It goes via a buffer amplifier and an analog switch to the input of the control amplifier. The analog switch is controlled by the signal, L_BAND_1, from the A12 PCB.
- LF_FM, from the A11 AM/FM Driver PCB, is the FM signal for the wide FM mode of operation. The wide FM mode of operation allows peak deviations of 100 MHz. This FM signal is fed to the control amplifier via a buffer amplifier and an analog switch. The analog switch is controlled by the signal, L_LFM, from the A12 PCB.

These signals are summed at the input of the control amplifier for the main tuning coil driver. This amplifier controls the driver that supplies the current for the main tuning coil. The main tuning coil current sense resistor senses the output current through the main coil and generates a feedback signal. The feedback signal is fed to the input of the control amplifier for the main tuning coil driver, where it is summed with the other input signals.

The main tuning coil driver uses –18V T regulated power to provide current for the main coil. At fast analog sweep speeds or during digital sweep stepping, –18V is not sufficient voltage to drive the inductance of the tuning coil. During these modes of operation, the voltage switches supply –43V T regulated power to the main tuning coil driver. This switching between –18V and –43V occurs automatically on demand.

In CW and narrow-band (≤100 MHz wide) analog sweep modes of operation, the signal, CW_FIL_1, closes an analog switch placing the CW filter network into the feedback path of the control amplifier for the main tuning coil driver. It also connects the FM tuning coil feedback signal to the control amplifier. The CW filter network reduces the bandwidth of the control amplifier to approximately 30 Hz. This reduced bandwidth improves the residual FM performance in the CW and narrow-band analog sweep modes.

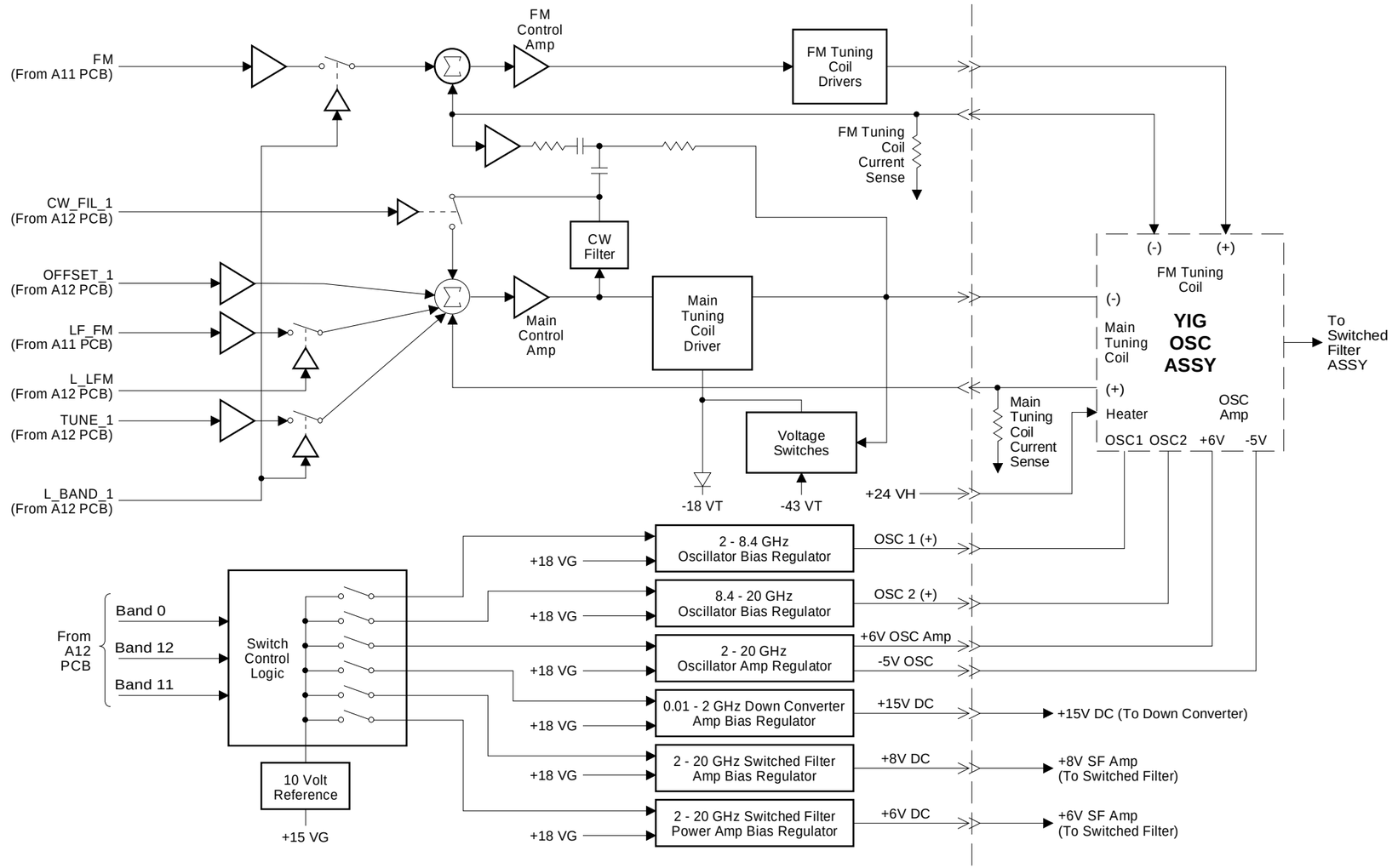


Figure 2-15. Block Diagram of the A13 YIG Driver PCB

Bias Supplies

The Band 0, Band 11, and Band 12 frequency band selection signals, from the A12 PCB, control the application of a +10V reference voltage to turn on the regulators that supply bias voltages to the YIG-tuned oscillator, the amplifiers in the switched filter, and the down converter. There are two oscillator bias regulators because the 2 to 20 GHz YIG-tuned oscillator is actually two oscillators with a common amplifier.

2 to 8.4 GHz Oscillator Bias

The Band 11 signal causes the +10V reference voltage to go to the 2 to 8.4 GHz oscillator bias regulator which supplies the 2 to 8.4 GHz portion of the YIG-tuned oscillator with +8V at 50 mA*.

8.4 to 20 GHz Oscillator Bias

The Band 12 signal causes the +10V reference voltage to go to the 8.4 to 20 GHz oscillator bias regulator which supplies the 8.4 to 20 GHz portion of the YIG-tuned oscillator with +8V at 50 mA*.

2 to 20 GHz Oscillator Amplifier Bias

Either the Band 11 or the Band 12 signal causes the +10V reference voltage to go to the 2 to 20 GHz oscillator amplifier regulator. This regulator supplies the 2 to 20 GHz amplifier located in the YIG-tuned oscillator with +6V at 150 mA* and –5V at 20 mA*.

2 to 20 GHz Switched Filter Amplifier Bias

Either the Band 11 or the Band 12 signal causes the +10V reference voltage to go to the 2 to 20 GHz switched filter amplifier bias regulator. This regulator supplies the preamplifier located in the switched filter with 8V at 150 mA*.

2 to 20 GHz Switched Filter Power Amp Bias

Either the Band 11 or the Band 12 signal causes the +10V reference voltage to go to the 2 to 20 GHz switched filter power amplifier bias regulator. This regulator supplies the power amplifier located in the switched filter with 6V at 400 mA*.

Down Converter Amplifier Bias

The Band 0 signal causes the +10V reference voltage to go to the 0.01 to 2 GHz down converter amplifier bias regulator. This regulator supplies the power amplifiers in the down converter with +15V at 600 mA*.

* All bias supply currents are approximate.

2-17 A14 DOUBLER DRIVER PCB

The A14 Doubler Driver PCB (Figure 2-16 on page 2-71) provides bias voltages and modulator drive signals for the three doubler/amplifiers located in the frequency extension unit. It also contains regulators that may be used in the future to supply bias voltages for a 40 to 60 GHz doubler/amplifier or a 2 to 20 GHz high power amplifier.

Bias Supplies

The Band 2, Band 3, Band 31, and Band 32 frequency band selection signals, from the A12 Analog Instruction PCB, control the application of a +10V reference voltage to turn on the regulators that supply bias voltages to the three doubler/amplifiers located in the FEU. The Band 4 and Band 5 frequency band selection signals control the application of the +10V reference voltage to turn on the bias regulators for the 40 to 60 GHz doubler/amplifier or the 2 to 20 GHz high power amplifier.

K Band Doubler Bias
The Band 2 signal causes the +10V reference voltage to go to the K Band (20 to 26.5 GHz) doubler bias regulator. This regulator supplies the K Band doubler/amplifier of the FEU with +12V at approximately 800 mA.

Ka1 Band Doubler Bias
The Band 31 signal causes the +10V reference voltage to go to the Ka1 Band (26.5 to 33 GHz) doubler bias regulator. This regulator supplies the Ka1 Band doubler/amplifier of the FEU with +12V at approximately 800 mA.

Ka2 Band Doubler Bias
The Band 32 signal causes the +10V reference voltage to go to the Ka2 Band (33 to 40 GHz) doubler bias regulator. This regulator supplies the Ka2 Band doubler/amplifier of the FEU with +12V at approximately 800 mA.

W Band Bias/2 to 20 GHz Power Amplifier Bias
When either a 40 to 60 GHz doubler/amplifier or a 2 to 20 GHz high power amplifier is installed in the instrument, the Band 4 signal causes the +10V reference voltage to go to the W Band (40 to 60 GHz) bias/2 to 20 GHz power amplifier bias regulator. This regulator supplies +8V at approximately 400 mA to either the W Band doubler/amplifier or the 2 to 20 GHz power amplifier (Bias A).

2 to 20 GHz Power Amplifier Bias
When a 2 to 20 GHz high power amplifier is installed in the instrument, the Band 5 signal causes the +10V reference voltage to go to the 2 to 20 GHz power amplifier bias regulators. These regulators supply +6V at approximately 150 mA (Bias B) and –5V at approximately 15 mA (Bias C) to the 2 to 20 GHz high power amplifier.

Modulator Shaper

As the doubler/amplifiers go into saturation, the linearity of the modulators change drastically at high power output levels. The modulator shaper corrects for this non-linearity by increasing the gain of the modulators at high power levels.

The ALC control signal, from the A10 ALC PCB, is fed to the shaper amplifier. As the doubler/amplifiers go into saturation, the gain of the shaper amplifier will begin to increase. In each frequency band, shaper amplifier gain is determined by the offset voltage for that particular frequency band. The Band 2, Band 3, Band 4, and Band 5 frequency band selection signals control the analog switch that provides a different offset voltage for each frequency band. YIG Offset DAC B, on the A12 Analog Instruction PCB, supplies a reference voltage (OFFSET_2) to fine tune the shaper amplifier gain for each frequency band. The YIG Offset DAC B settings for each frequency band are stored during calibration of the ALC for frequencies above 20 GHz.

Modulator Drivers

The Band 2, Band 3, Band 4, and Band 5 frequency band selection signals control the application of the shaper amplifier output to the modulator drivers for the doubler/amplifiers.

K Band Modulator Driver
The Band 2 signal causes the shaper amplifier output to go to the K Band (20 to 26.5 GHz) modulator driver. This driver supplies approximately +8.5 to +1V at approximately 100 to 250 mA to the modulator located in the K Band doubler/amplifier module of the FEU.

Ka Band Modulator Driver
The Band 3 signal causes the shaper amplifier output to go to the Ka Band (26.5 to 40 GHz) modulator driver. This driver supplies approximately +8.5 to +1V at approximately 100 to 250 mA to the modu-

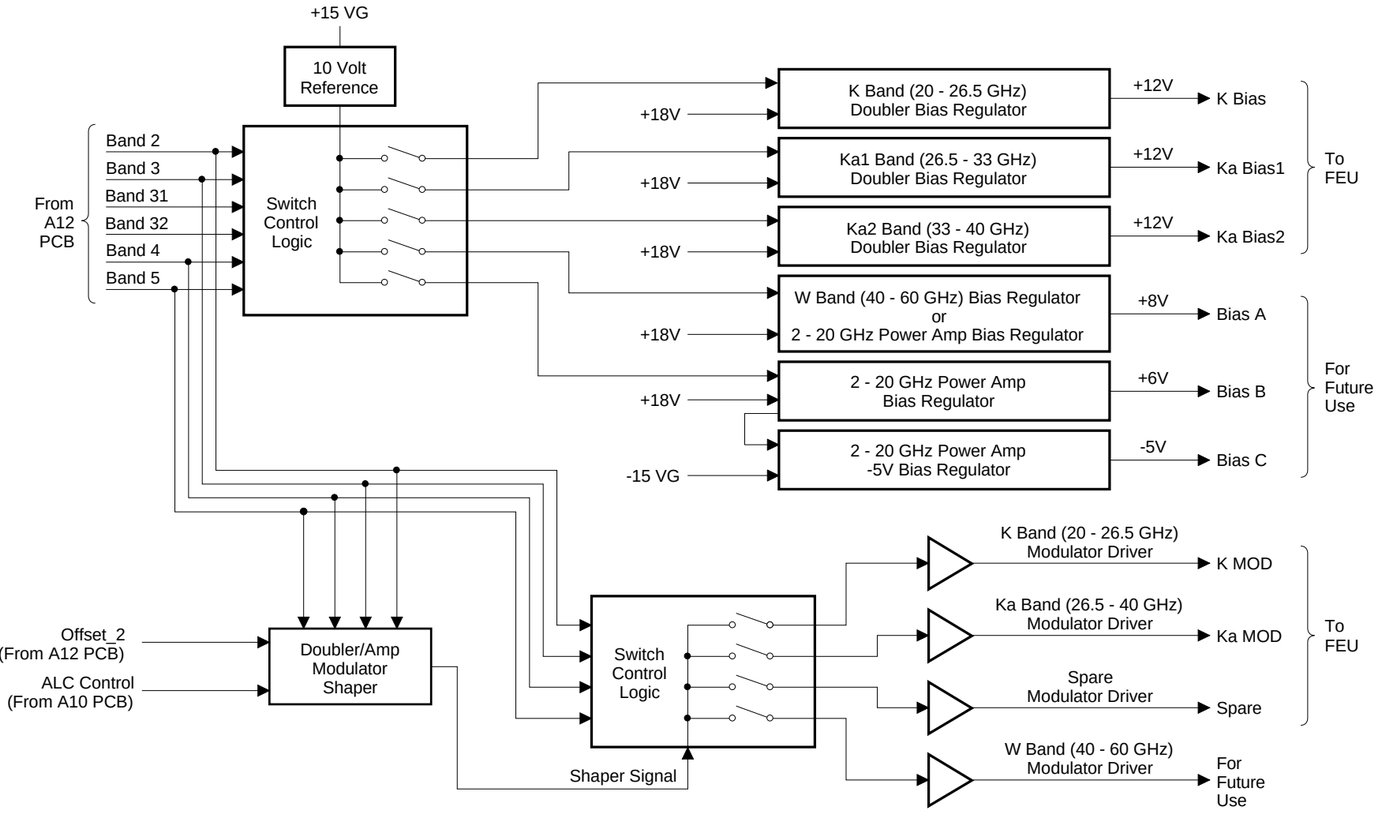


Figure 2-16. Block Diagram of the A14 Doubler Driver PCB

lators located in the Ka1 Band and Ka2 Band doubler/amplifier modules of the FEU.

W Band Modulator Driver
When a 40 to 60 GHz doubler/amplifier is installed in the instrument, the Band 4 signal causes the shaper amplifier output to go to the W Band (40 to 60 GHz) modulator driver. This driver supplies approximately +8.5 to +1V at approximately 100 to 250 mA to the modulator located in the W Band doubler/amplifier module.

Spare Modulator Driver
The Band 5 signal causes the shaper amplifier output to go to the spare modulator driver. This modulator driver is provided for future use.

2-18 A14-1 SDM DRIVER PCB

The A14-1 SDM Driver PCB (Figure 2-17) provides bias voltage for the doubler/amplifiers located in the Switched Doubler Module (SDM).

Bias Supply

The Band 2 and Band 3 frequency band selection signals, from the A12 Analog Instruction PCB, control the application of a +10V reference voltage to turn on the switched doubler module bias regulator. The regulator supplies the 20 to 40 GHz doubler/amplifiers of the SDM with +8V at approximately 975 mA.

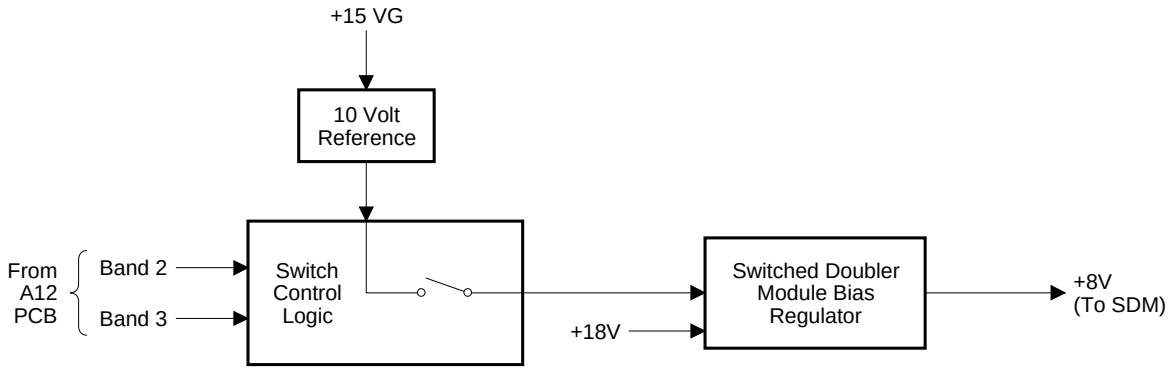


Figure 2-17. *Block Diagram of the A14-1 SDM Driver PCB*

2-19 A16 CPU INTERFACE PCB

The A16 CPU Interface PCB (Figure 2-18) contains circuitry to interface the CPU to various functions of the sweep generator. It contains the following circuitry:

- Rear Panel Signal Latches
- Dedicated Serial I/O
- Rotary Data Knob Decoder
- Digital Voltmeter
- Interrupt Control Circuits

CPU Interface

The A16 PCB is directly connected to the CPU via the main processor data bus (D0-D15). The circuit functions of the A16 PCB are addressed by the address bus lines, A01-A03, and the dedicated address lines, L_SEL6 and L_SEL7. The dedicated address line, L_SEL6, enables the address decoder that decodes the address lines, A01-A03, and provides strobes to (1) latch data from the data bus into the rear panel signals data latches and the DVM multiplexer data latch, and (2) enable the knob decoder, the DVM, the status data latch, and interrupt control circuits. The dedicated address line, L_SEL7, enables the address decoder that decodes the address lines, A01-A03, and supplies strobes to (1) latch data from the data bus into the serial I/O control latch and shift registers, and (2) control the clock/counter circuits.

Rear Panel Signals

Many of the rear panel signals for interfacing the sweep generator with other instruments are generated by the data latches on the A16 PCB. They include retrace/bandswitch blanking, markers, penlift control, sequential sync, and lock indicator output signals. The output signals, L_ALT_EN and L_ALT, go to the rear panel AUX I/O connector for use by the WILTRON 560A, 561, and 562 network analyzers in the alternate sweep mode of operation. The output signals, EOS_OUT and SWP_TRG, go to the rear panel AUX I/O connector for use as a hardware handshake when operating two 681XXAs in a master-slave mode. The CPU writes directly to these latches at the appropriate time for these signals.

Dedicated Serial I/O

The dedicated serial I/O circuitry provides a serial interface between the CPU and those circuits that are sensitive to a high-speed parallel data bus. This lets the CPU indirectly control the A2 Front Panel Control PCB, the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5 Fine Loop PCB, and the

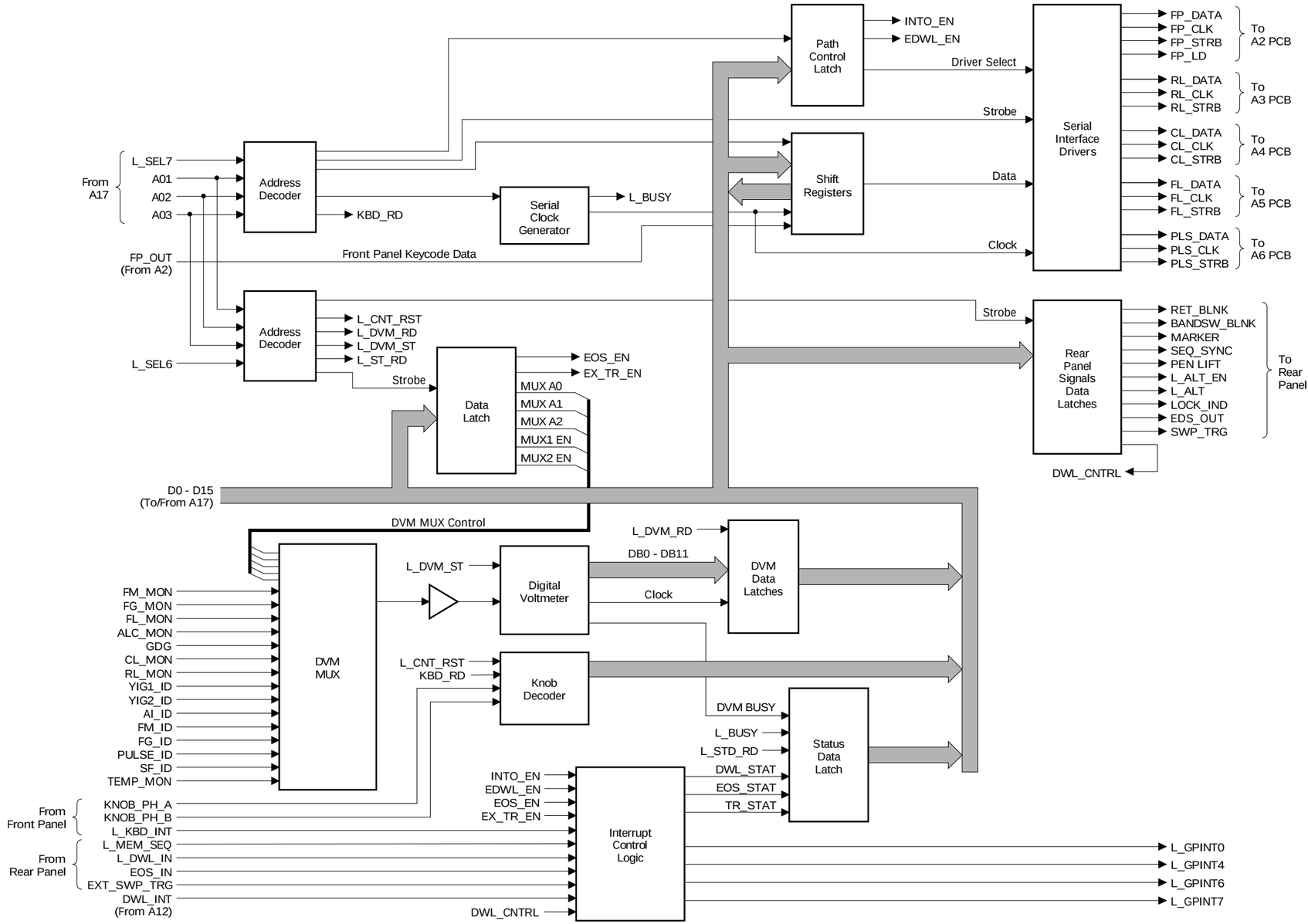


Figure 2-18. Block Diagram of the A16 CPU Interface PCB

A6 Square Wave Generator PCB. There is a separate serial data bus for each PCB.

Serial Output
The CPU first sends address and command data to set up the serial interface for the command/data transfer to the selected PCB. It then places the command/data information for the target PCB on the data bus. This 16-bit parallel command/data is clocked into the shift registers, where it is converted to a 16-bit serial data word format, then shifted out to the appropriate serial interface driver.

There are five serial interface drivers—one for each serial data bus. The selected driver is enabled by the driver select signal from the path control latch. The serial interface driver routes to the destination PCB (1) the serial command/data word, (2) the serial clock signal required to clock the command/data word into the destination serial-to-parallel converter, and (3) the strobe signal to load the converted command/data to the parallel data bus latches.

Serial Input
Whenever a key is pressed on the front panel, the A2 PCB generates an interrupt signal, L_KBD_INT, which goes via the A16 PCB to the CPU. When the CPU detects a keyboard interrupt, it sets up the serial data and clock interface for the A2 path. It also sends the signal, FP_LD, to the A2 PCB to strobe the parallel keycode data into the parallel-to-serial converter. The front panel clock signal then shifts the serial keycode data out via the serial data bus to the A16 PCB. The serial keycode data is clocked into the shift registers where it is converted to a parallel format and placed on the data bus. The CPU will then read the data and take appropriate action.

Knob Decoder

The knob decoder circuitry takes the phase A and phase B signals from the front panel rotary data knob optical encoder and converts them to a count that is proportional to the rate-of-turn of the knob. Whenever the rotary data knob is turned, with a parameter entry open, it generates the interrupt, L_GPINTO. This interrupt tells the CPU that it has data ready for it to read. In response, the CPU sends the strobe, L_CNT_RST, to the knob decoder. This signal places the data on the data bus and resets the counter. The CPU then reads the data.

DVM

The digital voltmeter (DVM) reads voltages from 16-channels for use in self test, calibration, and monitoring various functions of the sweep generator, such as %AM and FM deviation. The digital voltmeter is a 13-bit DVM with auto-polarity. It has a full scale range of ±10V and a conversion time of less than 30 µs. The DVM is calibrated using a 0V analog ground and the ±10V reference voltages from the A12 Analog Instruction PCB.

The CPU addresses the DVM multiplexer via a data latch to select which channel is to be measured. The output voltage from the selected channel goes via an absolute value circuit and a buffer amplifier to the DVM. The signal, L_DVM_ST, initiates DVM conversion of the analog voltage to a digital word. When the conversion is completed, the digital word is latched into the DVM data latches. The signal, L_DVM_RD, then places the digital word on the data bus where it is read and processed by the CPU.

Interrupt Control Circuits

The interrupt control circuits interface some of the sweep generator interrupts to the interrupt inputs of the CPU. The interrupt control circuits are enabled by signals from the CPU. When enabled, the following instrument interrupts cause the circuits to generate an interrupt to the CPU:

- Either L_KBD_INT, from the front panel, or L_MEM_SEQ, from the rear panel, produces the L_GPINT0 interrupt signal.
- L_DWL_IN, from the rear panel, produces the L_GPINT4 interrupt signal.
- Either DWL_INT, from the A12 PCB, or EOS_IN, from the rear panel, produces the L_GPINT6 interrupt signal.
- EXT_SWP_TRG, from the rear panel, produces the L_GPINT7 interrupt signal.

Some of the interrupts, such as EXT_SWP_TRG, are disabled when not in use. Some interrupt control circuits also supply an input to the status data latch for monitoring by the CPU.

Status Latch

The status latch is used to monitor the status of the DVM, the dedicated serial I/O, and certain interrupts. The signal, L_ST_RD, places the status latch data on the data bus where it can be read by the CPU.

2-20 A17 CPU PCB

The A17 CPU PCB (Figure 2-19) directly or indirectly controls all the main functions of the 681XXA. It contains the microprocessor and its supporting circuitry, CPU memory, address and data busses, a serial port interface, a parallel port interface, and a GPIB interface.

Microprocessor Circuits The CPU processor is a 16 MHz, Motorola 68000 microprocessor. The clock circuit, in conjunction with the crystal oscillator, generates the 16 MHz clock signal for the microprocessor. The microprocessor has a 16-bit data bus (D00-D15) and a 24-bit address bus (A01-A23). The address bus is used to address all memory locations and peripherals on the PCB. The control logic circuitry provides signals to enable all memory and peripherals.

CPU Memory The CPU memory is structured as follows:

- 512 Kbytes of EPROM that is used to store the main operating system components and instrument firmware.
- 32 Kbytes of EEPROM that is used to store calibration data for the instrument. This EEPROM is electrically eraseable and is programmed by the CPU during calibration.
- 32 Kbytes of non-volatile RAM that is used to store front panel setups in the power-off condition. A backup battery on the PCB powers the RAM during power off condition.
- 256 Kbytes of general purpose scratch-pad RAM.

Address Bus In addition to addressing all memory and peripherals on the PCB, the internal address bus goes to the address bus and dedicated address bus latches. The outputs of the address bus latch are the PCB address bus lines, A01-A04. The outputs of the dedicated address bus latch are the dedicated address lines L_SEL0 thru L_SEL7. These dedicated address lines are used in conjunction with the PCB address lines A01-A04 to select specific circuit functions located on the A9, A10, A11, A12, and A16 PCBs.

Data Bus Bi-directional transfer of data between the microprocessor, memory, and peripherals on the PCB takes place via the internal data bus, D00-D15, under the control of the microprocessor. The internal data bus is connected to data bus transceivers that provide an interface to the 681XXA main processor

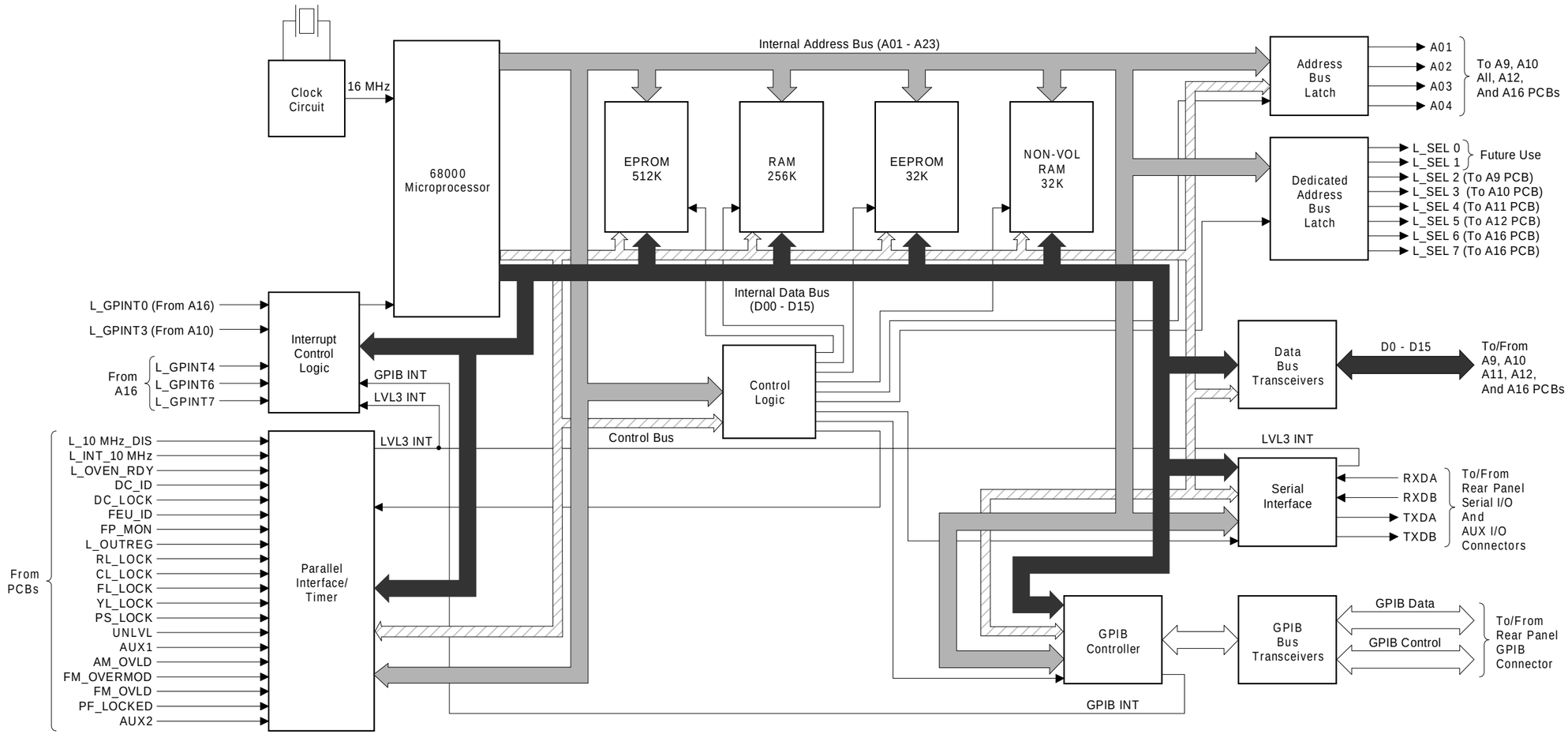


Figure 2-19. Block Diagram of the A17 CPU PCB

data bus, D0-D15. This allows bi-directional transfer of data between the CPU and the A9, A10, A11, A12, and A16 PCBs under the control of the microprocessor.

Parallel Interface/ Timer

The parallel interface port is used by the microprocessor to monitor the status of various operations and configurations of the sweep generator. The monitored operations include phase locking of the various loops, leveling of the ALC loop, AM and FM input signal levels, FM modulation level, voltage regulation, and crystal oscillator oven temperature. Configurations monitored include the presence of a down converter, a FEU, an external 10 MHz reference, and a high stability 10 MHz timebase.

The timer provides timing signals for wait periods controlled by the microprocessor. These wait periods trigger events and provide time for the phase-lock loops to achieve lock. During these waits, the microprocessor does other (non-related) tasks. At the end of a wait period, the timer sends an interrupt to the microprocessor via the interrupt control logic. The microprocessor then services the next (related) task.

Serial Interface

The serial interface circuit links the microprocessor to two RS-232 serial terminal ports. It provides parallel-to-serial and serial-to-parallel data conversion of bi-directional communication between the microprocessor and external devices. It sends an interrupt to the microprocessor via the interrupt control logic to request service.

GPIB Interface

The GPIB interface circuitry provides communication between the microprocessor and external devices via the IEEE-488 (GPIB) bus. It consists of the GPIB controller and bus transceivers.

The GPIB controller decodes command and data information from the GPIB bus and sends interrupts and data to the microprocessor. It also transmits data from the microprocessor to the GPIB bus under control of the microprocessor. The bus transceivers interface the controller to the GPIB bus and provide power-up/power-down bus protection.

Interrupt Control

In addition to processing on-board interrupts from the timer, serial interface, and GPIB controller circuits, the interrupt control logic circuit also processes the interrupt signals received from the A10 and A16 PCBs.

The interrupts from the A10 and A16 PCBs are described as follows:

- The L_GPINT0 interrupt signal from the A16 PCB occurs when either a front panel key is pressed or the external memory sequence signal is received from the sweep generator's rear panel.
- The L_GPINT3 interrupt signal from the A10 PCB occurs when an RF unleveled condition is reached.
- The L_GPINT4 interrupt signal from the A16 PCB occurs when an external dwell signal is received from the sweep generator's rear panel.
- The L_GPINT6 interrupt signal from the A16 PCB occurs when either a dwell signal, from the A12 Analog Instruction PCB, or an end-of-sweep signal, from the AUX I/O connector on the sweep generator's rear panel, is received. The end-of-sweep signal only occurs when operating two 681XXAs in a master-slave mode.
- The L_GPINT7 interrupt signal from the A16 PCB occurs when an external sweep trigger is received from the AUX I/O connector on the sweep generator's rear panel. This external sweep trigger only occurs when operating two 681XXAs in a master-slave mode.

2-21 A15, A18, & A19 POWER SUPPLY PCBs

The A15 Regulator PCB, A18 Power Supply PCB, and A19 AC Line Conditioner PCB, and part of the A21 Rear Panel PCB and Rear Casting Assembly make up the power supply subsystem (Figure 2-20). It provides all the regulated DC voltages used by the sweep generator circuits.

WARNING

Voltages hazardous to life are present throughout the power supply circuits, *even when the front panel* LINE *switch is in the* STANDBY *position*. When performing maintenance, use utmost care to avoid electrical shock.

Line Voltage Selector Module

The line voltage selector module, part of the rear casting assembly, contains the line voltage selector, EMI filter, and line fuses. The AC line voltage is fed via the EMI filter and line fuses to the line rectifier circuit. The line voltage selector is used to select 681XXA operation with either 115 Vac or 230 Vac line voltage.

Line Rectifier/ Doubler Circuit

The operation of the line rectifier circuit, located on the A21 Rear Panel PCB, is determined by the line voltage selector setting. In the 115 Vac setting, the circuit functions as a full-wave voltage doubler; in the 230 Vac setting, it functions as a full-wave bridge rectifier. In both modes of operation, the circuit produces a voltage output of +165 Vdc and –165 Vdc that is fed to the A19 Line Conditioner PCB.

The line rectifier circuit contains surge suppression thermistors and transient suppression varistors in its input and a transient suppression filter in its output. This output filter removes any 200 kHz switching transients returned from the switching transistors on the A19 PCB to prevent them from getting onto the AC power line.

A19 AC Line Conditioner PCB

The A19 AC Line Conditioner PCB contains the standby supply and the FET switching transistors for the main power supply. On the A19 PCB, the +165 Vdc and –165 Vdc voltage from the line rectifier has two paths. One path leads to the switching transistors; the other leads to the standby supply.

Standby Supply

The standby supply produces +30V which is fed via the A20 Motherboard PCB to the A15 Regulator

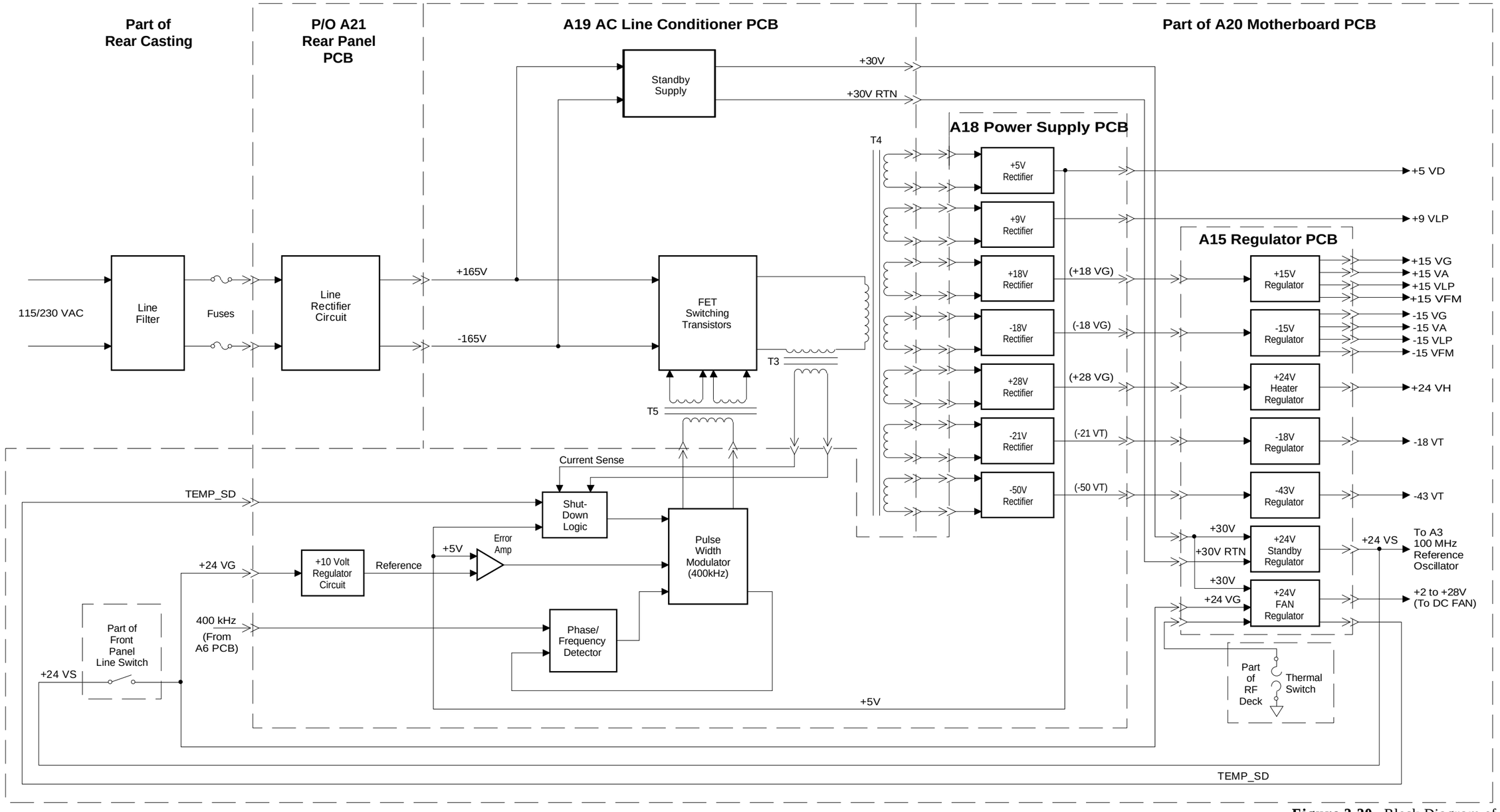


Figure 2-20. Block Diagram of the A15, A18, & A19 Power Supply PCBs

PCB. On the A15 PCB, the +30V is regulated to +24V (standby power).

Switching Transistors
The switching transistors are connected in a full bridge configuration and are the switching elements for the A18 Power Supply PCB. They alternately switch +165 Vdc and –165 Vdc to the primary windings of the main power transformer, T4, at a 200 kHz rate. Drive signals for the switching transistors are supplied by the gate drive transformer, T5, which receives its input from the pulse width modulator on the A18 PCB. Current sense transformer, T3, is used to monitor the primary current in T4. The current sense output is fed to the A18 PCB to provide a cycle-by-cycle current limit. The secondary windings of T4 produce reduced voltages that are routed to the A18 PCB where they are rectified and filtered.

A18 Power Supply PCB

The A18 Power Supply PCB contains the following circuits:

- pulse width modulator (PWM)
- phase/frequency detector
- 5V error amplifier
- shut down logic/soft start control
- low voltage rectifier/filter circuits

Pulse Width Modulator
The PWM generates two pulse trains with a variable duty cycle to drive the switching transistors. The duty cycle is determined by the amplitude of the control voltage applied to the PWM. During normal operation, the amplitude of the control voltage is determined by the output of the 5V error amplifier. During instrument power up (or fault recovery), it is controlled by the soft start control circuit. During abnormal conditions, it is controlled by the output of the shut down logic circuit.

Phase/Frequency Detector
The 400 kHz operating frequency of the PWM is phase locked by the phase/frequency detector. The 400 kHz reference signal, supplied by the A6 Square Wave Generator PCB, is fed to the phase/frequency detector where it is compared to the 400 kHz signal from the PWM. If there is a difference between the two signals, the detector generates a phase error signal to “pull” the PWM back on frequency.

In addition, the detector also supplies a signal that (1) goes to the CPU as PS_LOCK to indicate power supply phase lock and (2) causes an onboard LED to light when the PWM is phase locked.

5V Error Amplifier

The +5V output from the +5V rectifier/filter circuit goes to the 5V error amplifier. The other input to the error amplifier is a +5V reference voltage derived from the +10V regulator circuit. The error amplifier output varies the control voltage at the PWM. This causes the PWM to change the duty cycle of the drive signal to maintain the +5 VD output at precisely +5V.

Shut Down Logic/Soft Start Control Circuits

At start up, the +24V standby power is used to charge the soft start control capacitor. The voltage across the capacitor is sensed by the PWM, which causes it to set the duty cycle of the pulse train at its minimum. This causes the rectified outputs of the switching power supply to be at their minimum levels. As the capacitor continues charging, the duty cycle of the pulse train increases. This, in turn, causes the +5V supply output voltage (and other power supply outputs) to rise until it is regulated in the normal manner by the action of the 5V error amplifier.

The shut down logic circuit contains sensing circuitry that monitors the +5V supply output voltage, the current from the current sense transformer, and the TEMP_SD signal from a thermistor on the RF deck. When an overvoltage, overcurrent, or overtemperature condition occurs, the shut down logic circuit will generate a shut down pulse to the PWM, which turns off the switching transistors. The shut down pulse has a duration of less than one second. Upon reset, the power supply soft starts, as described above.

If the overvoltage, overcurrent, or overtemperature condition that started the above cycle is still present, the shut down logic circuit generates another pulse and again shuts down the power supply. This cycling will continue until either the overvoltage, overcurrent, or overtemperature condition is corrected or the unit is placed in STANDBY.

Rectifier/Filter Circuits
The reduced voltages from the secondary windings of T4 are rectified and filtered by full wave rectifiers and dual inductor/capacitor filter networks. The ±18 VG, +28 VG, –21 VT, and –50 VT output voltages are routed via the A20 Motherboard PCB to the A15 Regulator PCB. The +9 VLP output voltage goes via the A20 Motherboard PCB to the A3, A4, A5, A7, and A15 PCBs. The +5 VD output voltage is fed via the A20 Motherboard PCB to all digital circuits in the instrument. The +5V output voltage also goes to the input of the 5V error amplifier and the overvoltage sensing circuitry of the shut down logic circuit.

A15 Regulator PCB

The A15 Regulator PCB provides all of the regulated voltages for the sweep generator except for the +5V supply. All of the regulators are current limited and have foldback to reduce power consumption in case of a short circuit.

+24V Standby Power Supply
The unregulated +30 Vdc from the standby supply is connected to the input of the +24V standby regulator. This regulator supplies +23.33 ±0.5V for the 100 MHz reference oscillator oven heater, the front panel LINE switch circuitry, and the optional 10 MHz high stability time base. It is in operation any time the instrument is plugged into a power source. The regulator's output is designated as *+24 VS*; after the LINE switch, it is designated *+24 VG*.

+24V Fan Power Supply
The unregulated +30 Vdc from the standby supply is also connected to the input of the +24V fan regulator. This regulator provides voltage to drive the DC fan. The output voltage will vary from approximately +28V at 45°C to +10V at 0°C. The temperature is sensed by a thermister on the RF deck. If the switching power supply shuts down because of excessive temperature, the fan will continue to operate to cool the instrument.

+24V Heater Power Supply
This regulator supplies +24.32 ±0.5V for the YIG-tuned oscillator heaters, the V/GHz circuit on the analog instruction board, and coarse and fine loop circuits. When the instrument is switched to OPERATE, it also takes over the functions of the +24V

standby power supply. It gets its input voltage from the +28 VG unregulated supply on the A18 PCB. The output of this supply is designated as *+24 VH*.

+15V and –15V Power Supplies
The +18 VG and –18 VG voltages from the A18 PCB are reduced and regulated by the +15V and –15V regulators to produce the power supply outputs designated *±15 VG*, *±15 VA*, *±15 VFM*, and *±15 VLP*. These regulators have an output voltage tolerance of ±0.75V with current limiting at approximately 1.2A. The power supplies are divided into four groups to provide isolation between circuits, as follows:

- The ±15 VG supply provides voltages for the YIG driver, doubler driver, SDM driver, CPU, and CPU interface circuits and the switched filter and down converter assemblies.
- The ±15 VA supply provides voltages for the PIN control, ALC, AM/FM, and analog instruction circuits.
- The ±15 VFM supply provides voltage to the FM portion of the YIG driver circuits.
- The ±15 VLP provides voltages for the reference, coarse, fine, and YIG phase lock loop circuits.

–18V and –43V Power Supplies
The –18V regulator supplies current for the YIG-tuned oscillator main tuning coil during CW and slow analog sweeps. The output voltage, designated as *–18 VT*, is –18.06 ±0.36V and has a current capability of approximately 2.4A. The –18V regulator gets its input from the –21 VT unregulated supply on the A18 PCB.

The –43V regulator supplies current for the YIG-tuned oscillator main tuning coil during bandswitching, fast analog sweeps, and digital sweeps. The output voltage, designated as *–43 VT*, is –43.1 ±0.9V and has a current capability of approximately 1.2A. The –43V regulator gets its input from the –50 VT unregulated supply on the A18 PCB.

The –18V and –43V regulators are designed so that if the –18 VT supply is lost, it will automatically shut down the –43 VT supply.

Out of Regulation Circuit

The out of regulation circuit monitors all of the regulated power supply outputs. If any of the regulators has no output, the circuit will generate the signal, L_OUTREG. This signal goes to the CPU which will then display an error message during self test.

2-22 RF DECK ASSEMBLIES

The primary purpose of the RF deck assembly is to generate CW and swept frequency RF signals and route these signals to the front panel RF OUTPUT connector. It is capable of generating RF signals in the frequency range of 0.01 to 40 GHz.

The series 681XXA synthesized sweep generator uses a single 2 to 20 GHz YIG-tuned oscillator. All other frequencies are derived from the fundamental frequencies generated by this oscillator. RF output frequencies of 0.01 to 2 GHz are developed by downconverting the fundamental frequencies of 6.01 to 8 GHz (6.51 to 8.5 GHz for instruments with serial number 320001 and above). RF output frequencies of 20 to 40 GHz are produced by doubling the fundamental frequencies of 10 to 20 GHz.

The following paragraphs briefly describe the operation of the RF deck assembly components.

RF Deck Configurations

The configuration of the RF deck varies according to the sweep generator model and serial number. Block diagrams of the various RF deck configurations are shown in the following figures:

- Figure 2-21, page 2-93, is a block diagram of the RF deck assembly for models 68137A and 68147A with serial numbers below 320001.
- Figure 2-22, page 2-94, is a block diagram of the RF deck assembly for models 68163A and 68169A with serial numbers below 320001.
- Figure 2-23, page 2-99, is a block diagram of the RF deck assembly for models 68137A, 68147A, 68163A, and 68169A with serial number 320001 and above.

681XXA Model	Frequency Range
68137A	2-20 GHz
68147A	0.01-20 GHz
68163A	2-40 GHz
68169A	0.01-40 GHz

The block diagram of the RF deck shown in Figure 2-21 includes all of the common RF components found in a typical 681XXA RF deck assembly. Refer to this block diagram during the descriptions of common RF components presented below.

Common RF Components

Many RF components are common to all RF deck assembly configurations. These common RF components are described in the following paragraphs. RF components that are peculiar to a specific RF deck assembly configuration are described in later paragraphs as part of the description of that particular RF deck.

YIG-tuned Oscillator
The 2 to 20 GHz YIG-tuned oscillator actually contains two oscillators—one covering the frequency range of 2 to 8.4 GHz and one covering the frequency range of 8.4 to 20 GHz. Both oscillators use a common internal amplifier.

The YIG-tuned oscillator generates RF output signals that have low broadband noise and low spurious content. It is driven by the FM and Main tuning coil currents and bias voltages from the A13 YIG Driver PCB. During CW mode, the main tuning coil current tunes the oscillator to within a few megahertz of the final output frequency. The phase-lock circuitry of the YIG loop then fine adjusts the oscillator's FM tuning coil current to make the output frequency exact.

During broad-band analog frequency sweeps (>100 MHz wide), the main tuning coil current tunes the oscillator through the sweep frequency range. Phase locking to fine adjust the oscillator's output frequency is only done at the bottom and top of the sweep ramp and on both sides of each band switch point. Narrow-band analog frequency sweeps (≤100 MHz wide) are accomplished by summing the appropriate sweep ramp signal into the oscillator's FM tuning coil control path. The YIG-tuned oscillator's RF output is then swept about a center frequency that is set by the main tuning coil current. Phase locking to fine tune the output frequency is done at the center frequency of the sweep. Frequency modulation of the RF output is also accomplished by summing the external modulating signals into the oscillator's FM tuning coil control path.

Switched Filter Assembly
The switched filter assembly contains RF amplifiers, a modulator, switched low-pass filters, and RF pick offs.

In the switched filter assembly, the RF output signal from the YIG-tuned oscillator is fed via RF amplifiers and the modulator to the switched low-pass filters. The RF amplifiers are used to increase the power level of the signal and the modulator is used to control its power level. A portion of the RF signal input to the modulator is picked off and coupled out

via connector J5 to the Sampler for use by the YIG loop circuitry.

The modulator control input provides a signal to the modulator to control the power level of the RF output signals. This modulator control signal is received from the A9 PIN Control PCB, where it is derived from the A10 PCB's ALC control signal input. Amplitude modulation of the RF output signal is accomplished by varying the modulator control drive signal with the external modulation signal. Square wave modulation of the the RF output signal is accomplished by turning the RF output signal on and off using internally generated square wave or external square wave inputs to control the modulator control signal.

The RF signal from the modulator is fed via PIN switches to connector J3 and the switched low-pass filters. The PIN switches receive their drive current from the A9 PIN Control PCB. Connector J3 is used to output those fundamental frequencies that are used by the down converter to generate 0.01 to 2 GHz RF signals. The low-pass filters provide rejection of the harmonics that are generated by the YIG-tuned oscillator.

After routing through the appropriate filtering path, the 2 to 20 GHz RF signal is multiplexed by the PIN switches to the switched filter output J2. The 0.01 to 2 GHz RF signal is received from the down converter at connector J1, then multiplexed through to the switched filter output.

Directional Coupler

The directional coupler transfers the RF output signals to the sweep generator's RF OUTPUT connector. It also couples a portion of the RF output signal to an internal RF detector. The detector output is coupled out as a feedback signal input to the internal power leveling circuitry located on the A10 ALC PCB.

Step Attenuator

The optional step attenuator provides up to 110 dB attenuation of the RF output in 10 dB steps. The step attenuator drive current is supplied by the A9 or A9-1 PIN Control PCB.

RF Decks for Models Having Serial Numbers Below 320001

The RF deck assemblies for models 68137A, 68147A, 68163A, and 68169A having serial numbers below 320001 are described in the following paragraphs. Refer to the block diagrams in Figures 2-21 and 2-22 during the following descriptions.

Power Level Control and Modulation

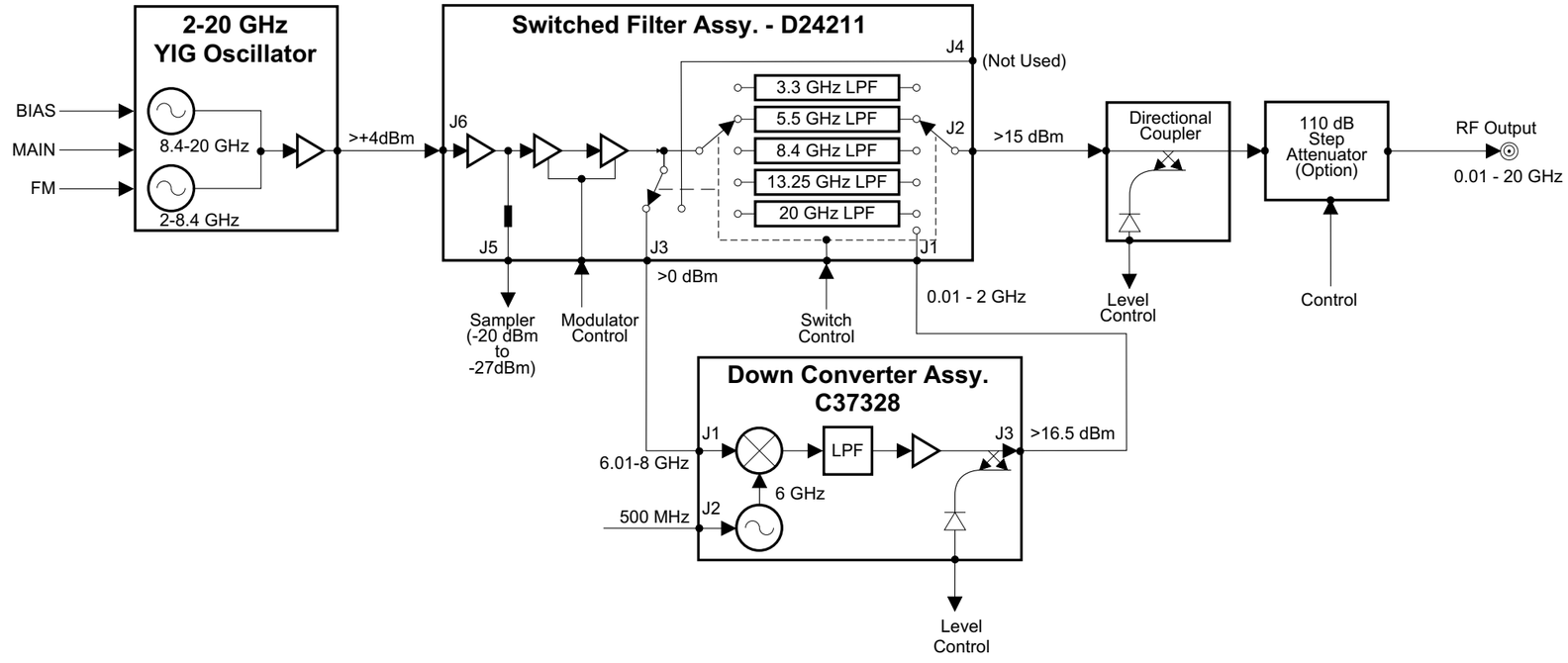
The RF output signal from the YIG-tuned oscillator is fed to connector J6 on the switched filter assembly. In the switched filter assembly, the RF signal is amplified then goes to the modulator. A portion of the RF signal to the modulator is picked off and coupled out via connector J5 to the Sampler for use by the YIG loop circuitry. The modulator controls the power level of the RF output signals. The modulator control signal is received from the A9 PCB where it is developed from the ALC control signal. The modulator is also used for AM and square wave modulation of the RF output signal.

RF Signal Filtering

The RF signal from the modulator is fed via PIN switches to connectors J3 and J4 and the switched low-pass filters. PIN switch drive current is received from the A9 PCB. Connector J3 is used in models 68147A and 68169A to output the 6.01 to 8 GHz RF signal that is used by the down converter. Connector J4 is used in models 68163A and 68169A to output the 10 to 20 GHz RF signal that is used by the frequency extension unit. The switched low-pass filters provide rejection of the harmonics that are generated by the YIG-tuned oscillator. The 2 to 20 GHz RF signal from the modulator has five filtering paths; 3.3 GHz, 5.5 GHz, 8.4 GHz, 13.25 GHz, and 20 GHz.

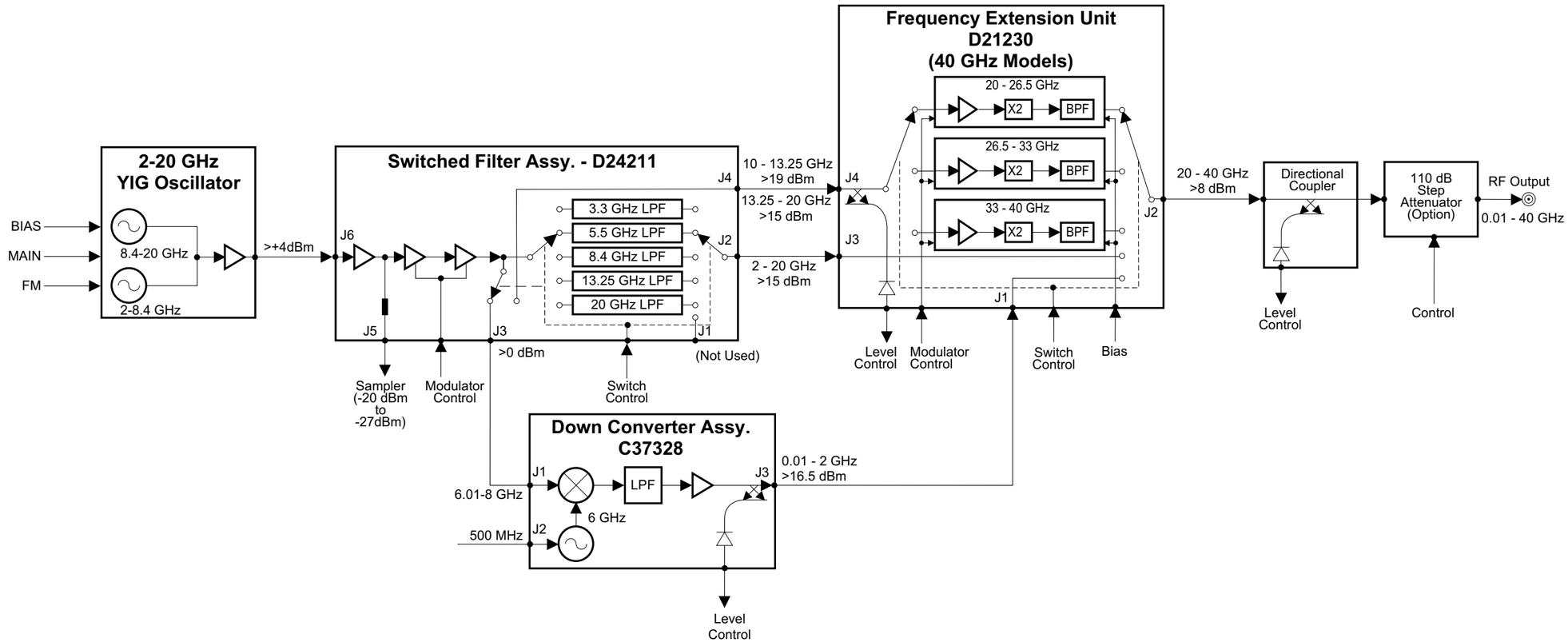
After routing through the appropriate filtering path, the 2 to 20 GHz RF signal is multiplexed by the PIN switches to the switched filter assembly output at connector J2. In the model 68147A, the 0.01 to 2 GHz RF signal, from the down converter, is received at connector J1, then multiplexed through to the switched filter output (Figure 2-21).

From J2, the RF signal goes to either the directional coupler (models 68137A and 68147A) or the input connector J3 on the frequency extension unit (models 68163A and 68169A).



NOTE
Down Converter Assy not installed in Model 68137A

Figure 2-21. Block Diagram of the RF Deck Assembly for Models 68137A and 68147A with serial numbers below 320001.



NOTE
Down Converter Assy not installed in Model 68163A

Figure 2-22. Block Diagram of the RF Deck Assembly for Models 68163A and 68169A with serial numbers below 320001.

Down Converter

The 0.01 to 2 GHz Down Converter, found in models 68147A and 68169A, contains a 6 GHz VCO that is phase-locked to the 500 MHz reference signal from the A3 Reference Loop PCB. The 6 GHz VCO's phase-lock condition is monitored by the CPU. The 6 GHz VCO is on at all times; however, the down converter amplifier is powered on by the A13 YIG Driver PCB only when the 0.01 to 2 GHz frequency range is selected.

During CW or swept frequency operations in the 0.01 to 2 GHz frequency range, the 6.01 to 8 GHz RF signal output from J3 of the switched filter assembly goes to input connector J1 of the down converter. The 6.01 to 8 GHz RF signal is then mixed with the 6 GHz VCO signal resulting in a 0.01 to 2 GHz RF signal. The resultant RF signal is fed through a 2 GHz low-pass filter, then amplified and routed to the output connector J3. A portion of the down converter's RF output signal is detected and coupled out for use in internal leveling. The detected RF sample, along with a resistance representing the down converter's temperature, is routed to the A10 ALC PCB.

In the model 68147A, the 0.01 to 2 GHz RF output from the down converter goes to input connector J1 of the switched filter assembly(Figure 2-21). There, the 0.01 to 2 GHz RF signal is multiplexed into the switched filter's output path.

In the model 68169A, the 0.01 to 2 GHz RF output from the down converter goes to input connector J1 of the frequency extension unit (Figure 2-22). There, the 0.01 to 2 GHz RF signal is multiplexed into the FEU's output path.

Frequency Extension Unit

The frequency extension unit (FEU), found in models 68163A and 68169A, is used to double the fundamental frequencies of 10 to 20 GHz to produce RF output frequencies of 20 to 40 GHz. Refer to the block diagram in Figure 2-22 during the following description.

During CW or swept frequency operations in the 20 to 40 GHz frequency range, the 10 to 20 GHz RF signal output from J4 of the switched filter assembly goes to J4 of the FEU. A portion of the 10 to 20 GHz

RF signal input to the FEU is detected and coupled out to the FEU ALC modulator driver circuit on the A9 PCB. The resulting modulator control signal goes to the modulator in the switched filter assembly to adjust the power level of the RF input to the FEU. In the 20 to 26.5 GHz frequency range, the FEU requires +18 dBm RF input power; in the 26.5 to 40 GHz frequency range, the FEU requires +16 dBm RF input power. These power levels prevent overloading of the FEU doublers.

In the FEU, the 10 to 20 GHz RF signal is routed by PIN switches to the doubler/amplifiers. PIN switch drive current is received from the A9 PCB. There are three doubler/amplifier paths, each with its own bandpass filter to maintain good harmonic performance. The frequency ranges of the three paths are 20 to 26.5 GHz, 26.5 to 33 GHz, and 33 to 40 GHz. Bias voltages and modulator control signals for the doubler/amplifiers are provided by the A14 Doubler Driver PCB. The ALC control signal from the A10 PCB goes to the modulator driver circuitry on the A14 PCB. The resulting modulator control signal is fed to each doubler/amplifier to adjust the RF output level for the 20 to 40 GHz portion of the frequency band.

After routing through the appropriate doubler/amplifier path, the 20 to 40 GHz RF signal is multiplexed by the PIN switches to the FEU output at connector J2. The 2 to 20 GHz RF signal is input from the switched filter assembly at connector J3, then multiplexed through to the FEU output. In the model 68169A, the 0.01 to 2 GHz RF signal is input from the down converter at connector J1, then multiplexed through to the FEU output.

Power Level Detection/ALC Loop

The RF signal output from either the switched filter assembly (models 68137A and 68147A) or the FEU (models 68163A and 68169A) goes to the directional coupler for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A10 ALC PCB. In these circuits, the signal from the detector is summed with the reference voltage that represents the desired RF output power level. The resulting voltage is fed from the A10 PCB to the ALC modulator driver circuit on the A9 PCB (and A14 PCB for models 68163A and 68169A). The re-

sulting modulator control signal goes to the modulator in the switched filter assembly to adjust the RF output power level.

RF Decks for Models with Serial Number 32001 and Above

The RF deck assemblies for models 68137A, 68147A, 68163A, and 68169A having serial number 320001 and above are described in the following paragraphs. Refer to the block diagram in Figure 2-23, on page 2-99, during the following descriptions.

Power Level Control and Modulation

The RF output signal from the YIG-tuned oscillator is fed to connector J6 on the switched filter assembly. In the switched filter assembly, the RF signal is amplified then goes to the modulator. A portion of the RF signal to the modulator is picked off and coupled out via connector J5 to the Sampler for use by the YIG loop circuitry. The modulator controls the power level of the RF output signals. The modulator control signal is received from the A9-1 PCB where it is developed from the ALC control signal. The modulator is also used for AM and square wave modulation of the RF output signal.

RF Signal Filtering

The RF signal from the modulator is fed via PIN switches to the switched low-pass filters. PIN switch drive current is received from the A9-1 PCB. A coupler in the switched filter path provides the RF signal for the down converter. Whenever the models 68147A and 68169A are generating RF signals in the 0.01 to 2 GHz frequency range, a 6.51 to 8.5 GHz RF signal is coupled out, through a 8.5 GHz low-pass filter, and routed to the down converter. The switched low-pass filters provide rejection of the harmonics that are generated by the YIG-tuned oscillator. The 2 to 20 GHz RF signal from the modulator has four filtering paths and a through path. The four filtering paths are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz. Signals above 13.5 GHz are routed via the through path.

After routing through the appropriate path, the 2 to 20 GHz RF signal is multiplexed by the PIN switches to the switched filter assembly output at connector J2. The 0.01 to 2 GHz RF signal, from the down converter, is received at connector J1, then multiplexed through to the switched filter output.

From J2, the RF signal goes via a 20 GHz low-pass filter to either the directional coupler (models 68137A and 68147A) or the input connector J1 on the switched doubler module (models 68163A and 68169A).

Down Converter

The 0.01 to 2 GHz Down Converter, found in models 68147A and 68169A, contains a 6.5 GHz VCO that is phase-locked to the 500 MHz reference signal from the A3 Reference Loop PCB. The 6.5 GHz VCO's phase-lock condition is monitored by the CPU. The 6.5 GHz VCO is on at all times; however, the down converter amplifier is powered on by the A13 YIG Driver PCB only when the 0.01 to 2 GHz frequency range is selected.

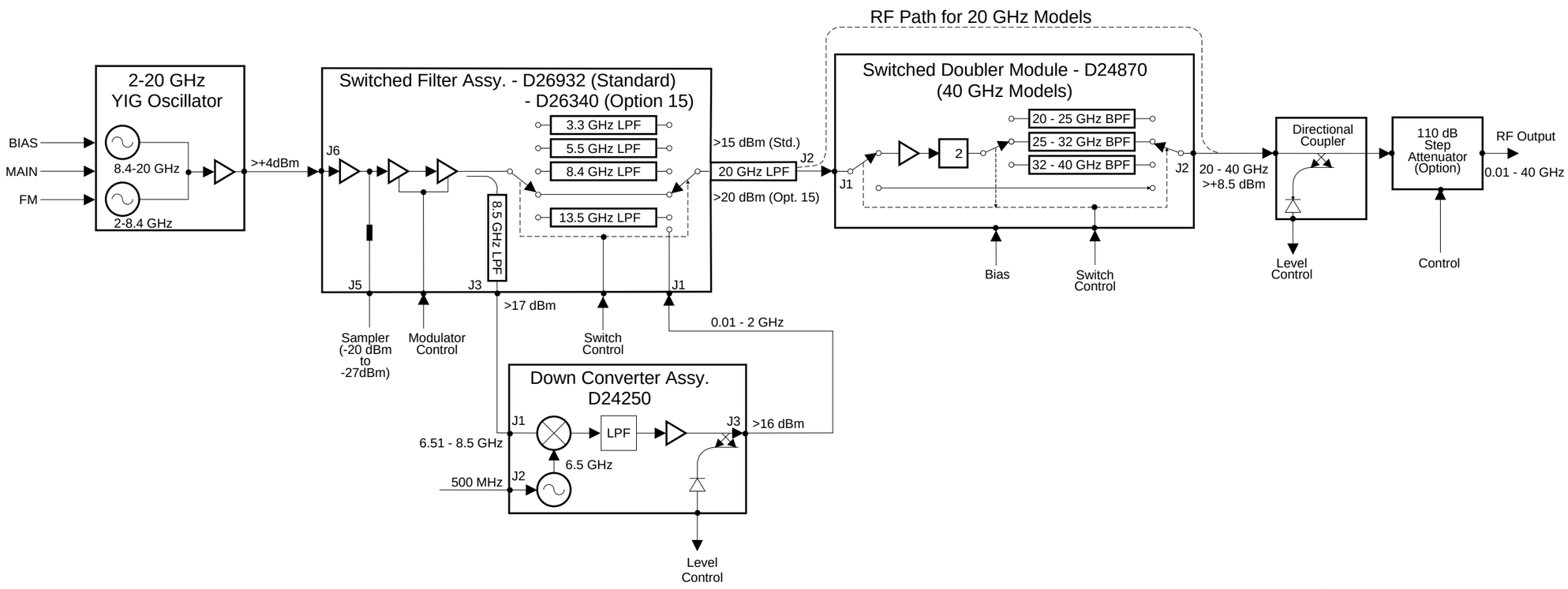
During CW or swept frequency operations in the 0.01 to 2 GHz frequency range, the 6.51 to 8.5 GHz RF signal output from J3 of the switched filter assembly goes via a 20 dB attenuator to input connector J1 of the down converter. The 6.51 to 8.5 GHz RF signal is then mixed with the 6.5 GHz VCO signal resulting in a 0.01 to 2 GHz RF signal. The resultant RF signal is fed through a 2 GHz low-pass filter, then amplified and routed to the output connector J3. A portion of the down converter's RF output signal is detected and coupled out for use in internal leveling. The detected RF sample, along with a resistance representing the down converter's temperature, is routed to the A10 ALC PCB.

The 0.01 to 2 GHz RF output from the down converter goes to input connector J1 of the switched filter assembly. There, the 0.01 to 2 GHz RF signal is multiplexed into the switched filter's output path.

Switched Doubler Module

The switched doubler module (SDM), found in models 68163A and 68169A, is used to double the fundamental frequencies of 10 to 20 GHz to produce RF output frequencies of 20 to 40 GHz.

The RF signal from the switched filter assembly is input to the SDM at J1. During CW or swept frequency operations in the 20 to 40 GHz frequency range, the 10 to 20 GHz RF signal input is routed by PIN switches to the doubler/amplifiers. PIN switch drive current is provided by the A9-1 PCB and bias voltage for the doubler/amplifiers is sup-



NOTES

1. Down Converter Assy not installed in Models 68137A and 68163A.

2. Switched Doubler Module not installed in Models 68137A and 68147A.

Figure 2-23. Block Diagram of the RF Deck Assembly for Models 68137A, 68147A, 68163A, and 68169A with serial number 320001 and above.

plied by the A14-1 SDM Driver PCB. The RF signal is amplified, then doubled in frequency. From the doubler, the 20 to 40 GHz RF signal is routed by PIN switches to the bandpass filters. There are three bandpass filter paths to provide good harmonic performance. The frequency ranges of the three paths are 20 to 25 GHz, 25 to 32 GHz, and 32 to 40 GHz.

After routing through the appropriate bandpass filter path, the 20 to 40 GHz RF signal is multiplexed by the PIN switches to the SDM output at connector J2. RF signals input to the SDM of ≤20 GHz are multiplexed through by the PIN switches to output connector J2.

Power Level Detection/ALC Loop

The RF signal output from either the switched filter assembly (models 68137A and 68147A) or the SDM (models 68163A and 68169A) goes to the directional coupler for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A10 ALC PCB. In these circuits, the signal from the detector is summed with the reference voltage that represents the desired RF output power level. The resulting voltage is fed from the A10 PCB to the ALC modulator driver circuit on the A9-1 PCB. The resulting modulator control signal goes to the modulator in the switched filter assembly to adjust the RF output power level.

Chapter 3
Performance Verification

Table of Contents

Chapter 3
Performance Verification

3-1 INTRODUCTION

This chapter contains tests that can be used to verify the performance of the Series 681XXA Synthesized Sweep Generator to specifications. These tests support all instrument models having any version of firmware. Units with Option 2 (110 dB step attenuator), Option 11 (0.1 Hz frequency resolution), and Option 15 (high power output) are also covered.

3-2 RECOMMENDED TEST EQUIPMENT

Table 3-1 (page 3-4) provides a list of the recommended test equipment for the performance verification tests.

The test procedures refer to specific test equipment front panel control settings when the test setup is critical to making an accurate measurement. In some cases, the user may substitute test equipment having the same critical specifications as those on the recommended test equipment list.

Contact your local WILTRON service center (refer to Table 1-5 on page 1-15) if you need clarification of any equipment or procedural reference.

3-3 TEST RECORDS

A blank copy of a sample performance verification test record for each 681XXA model is provided in Appendix A. Each test record contains the model-specific variables called for by the test procedures. It also provides a means for maintaining an accurate and complete record of instrument performance. We recommend that you copy these pages and use them to record the results of your initial testing of the instrument. These initial test results can later be used as benchmark values for future tests of the same instrument.

3-4 CONNECTOR AND KEY LABEL NOTATION

The test procedures include many references to equipment interconnections and control settings. For all 681XXA references, specific labels are used to denote the appropriate menu key, data entry key, data entry control, or connector (such as CW/SWEEP SELECT or RF OUTPUT). Most references to supporting test equipment use general labels for commonly used controls and connections (such as Span or RF Input). In some cases, a specific label is used that is a particular feature of the test equipment listed in Table 3-1.

Table 3-1. *Recommended Test Equipment for Performance Verification Tests*

INSTRUMENT	CRITCAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	TEST NUMBER
Spectrum Analyzer, with Diplexer Assy and External Mixers	*Frequency Resolution:* 0.01 to 40 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794, with External Mixers: WM780K (18 to 26.5 GHz) WM780A (26.5 to 40 GHz) Diplexer Assy: 015--385-00	3-7, 3-8
Spectrum Analyzer	*Frequency Range:* 20 Hz to 40 MHz *Resolution Bandwidth:* ≤3 MHz	Hewlett-Packard, Model 3585B	3-9
Frequency Counter with External Mixer	*Frequency Range:* 0.01 to 40 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz *Other:* External Time Base Input	EIP Microwave, Inc. Model 578A, with External Mixer: Option 91 (26.5 to 40 GHz)	3-6
Power Meter, with Power Sensor	*Power Range:* –30 to +20 dBm (1μW to 100mW)	Hewlett-Packard Model 436A, with Power Sensor: HP 8487A (0.01 to 50 GHz)	3-10
Frequency Standard	*Frequency:* 10 MHz *Accuracy:* 1 x 10^{-10} parts/day	Spectracom Corp., Model 8161	3-5
Oscilloscope	*Bandwidth:* DC to 150 MHz *Vertical Sensitivity:* 2mV/division *Horizontal Sensitivity:* 50 ns/division	Tektronix, Inc. Model 2445	3-5, 3-10
Mixer	*Frequency Range:* 1 to 26 GHz	RHG Electronics Laboratory, Inc. Model DMS1-26A	3-9
Adapter	K (male) to 2.4 mm (female) Adapts the Power Sensor, HP 8487A, to the 681XXA RF OUTPUT connector	Hewlett-Packard Part Number: HP 11904D	3-10
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* .+17 dBm *Attenuation:* 10 dB	WILTRON, Model 41KC-10	3-8, 3-9
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 20 dB	WILTRON, Model 41KC-20	3-8
Tee	*Connectors:* 50Ω BNC	Any common source	3-9
Cables	*Connectors:* 50Ω BNC	Any common source	All tests

3-5 INTERNAL TIME BASE AGING RATE TEST (OPTIONAL)

The following test can be used to verify that the 681XXA 10 MHz time base is within its aging specification. The 681XXA derives its frequency accuracy from an internal 100 MHz crystal oscillator standard. (With Option 16 installed, frequency accuracy is derived from an internal high-stability 10 MHz crystal oscillator.) An inherent characteristic of crystal oscillators is the effect of crystal *aging* within the first few days to weeks of operation. Typically, the crystal oscillator's frequency increases slightly at first, then settles to a relatively constant value for the rest of its life. The 681XXA reference oscillator aging is specified as $<1x10^{-7}$ parts per day ($<5x10^{-10}$ with Option 16).

NOTE

Do not confuse crystal aging with other short term frequency instabilities: i.e., noise and temperature. The internal time base of the instrument may not achieve its specified aging rate before the specified warm-up time of 7 to 30 days has elapsed; therefore, this performance test is optional.

For greatest absolute frequency accuracy, allow the 681XXA to warm up until its RF output frequency has stabilized (usually 7 to 30 days). Once stabilized, the change in reference oscillator frequency should remain within the aging rate if; (1) the time base oven is not allowed to cool, (2) the instrument orientation with respect to the earth's magnetic field is maintained, (3) the instrument does not sustain any mechanical shock, and (4) ambient temperature is held constant. This test should be performed upon receipt of the instrument and again after a period of several days to weeks to fully qualify the aging rate.

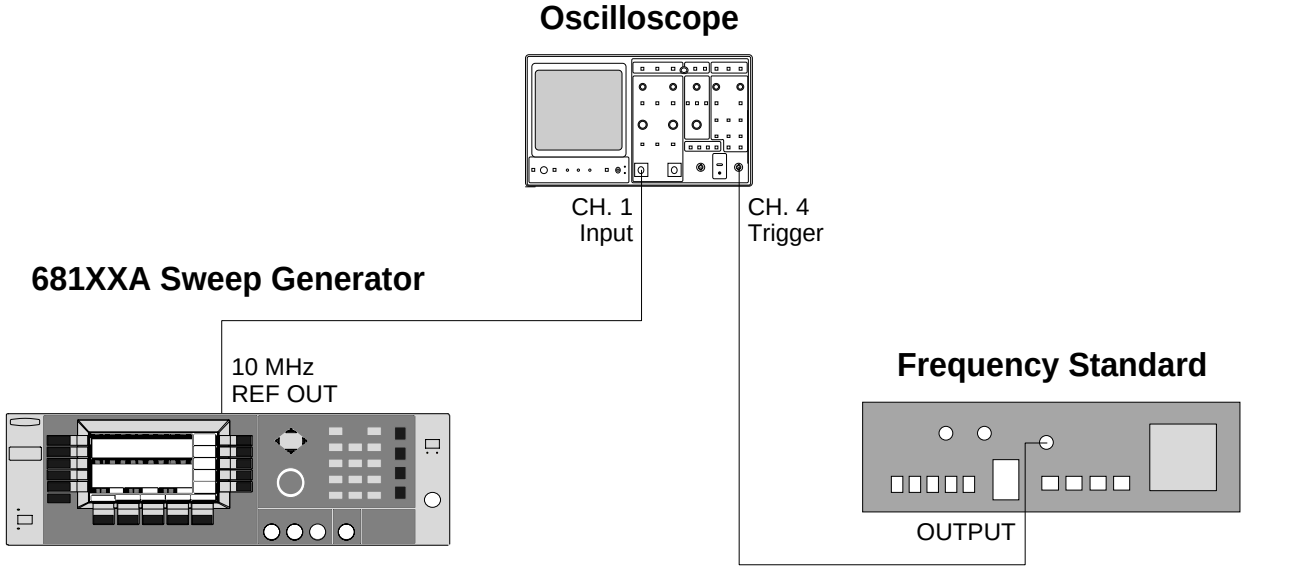


Figure 3-1. *Equipment Setup for Internal Time Base Aging Rate Test*

Test Setup

Connect the equipment, shown in Figure 3-1, as follows:

1. Connect the 681XXA rear panel 10 MHz REF OUT to the Oscilloscope vertical input.

2. Connect the output of the Frequency Standard (having a long term stability of $\leq 1x10^{-10}$) to the Oscilloscope external trigger input.

3. Set the Oscilloscope controls as follows:
   a. TRIGGER on CH.1
   b. TIME/DIV: 50 ns
   c. VOLT/DIV: 0.5

NOTE

Before beginning this procedure, *always* let the 681XXA warm up for a minimum of 120 hours (72 hours for instruments with Option 16). Failure to do so can cause inaccurate aging rate measurements.

Test Procedure

The time (in seconds) required for a specific phase change of 1 cycle (360°) is measured at the start and finish of the test time period (at least 3 but preferably 24 hours or more). Aging rate is then calculated with a formula that (inversely) relates time and frequency.

1. Adjust the Oscilloscope external triggering controls for a stable display of the 681XXA 10 MHz REF OUT signal.

2. Record the start time of the test period as T_S on the Test Record for the model being tested.

3. Measure the time (in seconds) required for a 360° phase change to occur on the Oscilloscope display. Record this as T_1 on the Test Record.

4. Wait for a period of time (at least 3 but preferably 24 hours) and remeasure the time required for a 360° phase change. Record this as T_2 on the Test Record.

5. Immediately record the finish time of the test period as T_F on the Test Record.

6. Calculate the aging rate using the following formula (refer to the example at the end of the procedure):

$$Aging\ Rate = \left(\frac{1 cycle}{F_{STD}}\right) x \left(\left|\frac{1}{T_1} - \frac{1}{T_2}\right|\right) x \left(\frac{T_{SPEC}}{TP}\right)$$

Where:
1 cycle = Phase change reference for the time measurement (360°)
F_{STD} = $10x10^6$ Hertz (10 MHz Time Base)
T_1 = Initial 360° phase change time (seconds)
T_2 = Final 360° phase change time (seconds)
T_{SPEC} = Spec. reference period (i.e., per day)
TP = Test period (hours) = $T_F - T_S$
T_F = Test period end time (hours)
T_S = Test period start time (hours)

7. Record the computed result on the Test Record. To meet the specification, the calculated aging rate must be $<1x10^{-7}$ per day ($<5x10^{-10}$ per day with Option 16).

EXAMPLE: At the beginning of the test, the time for a 360° phase change to occur was measured at 30 seconds.
T_1 = 30 (seconds)

After a test period of 24 hours, the time required for a 360° phase change to occur is measured at 32 seconds.
T_2 = 32 (seconds)
TP = 24 (hours)

$$Aging\ Rate = \left(\frac{1}{10\ x\ 10^6}\right) x \left(\left|\frac{1}{30} - \frac{1}{32}\right|\right) x \left(\frac{24}{24}\right)$$

$$= (1 \times 10^{-7}) \times (2.08 \times 10^{-3}) \times 1$$

$$= 2.08 \times 10^{-10}$$

3-6 FREQUENCY SYNTHESIS TESTS

The following tests can be used to verify correct operation of the frequency synthesis circuits. Frequency synthesis testing is divided into two parts—coarse loop/YIG loop tests and fine loop tests.

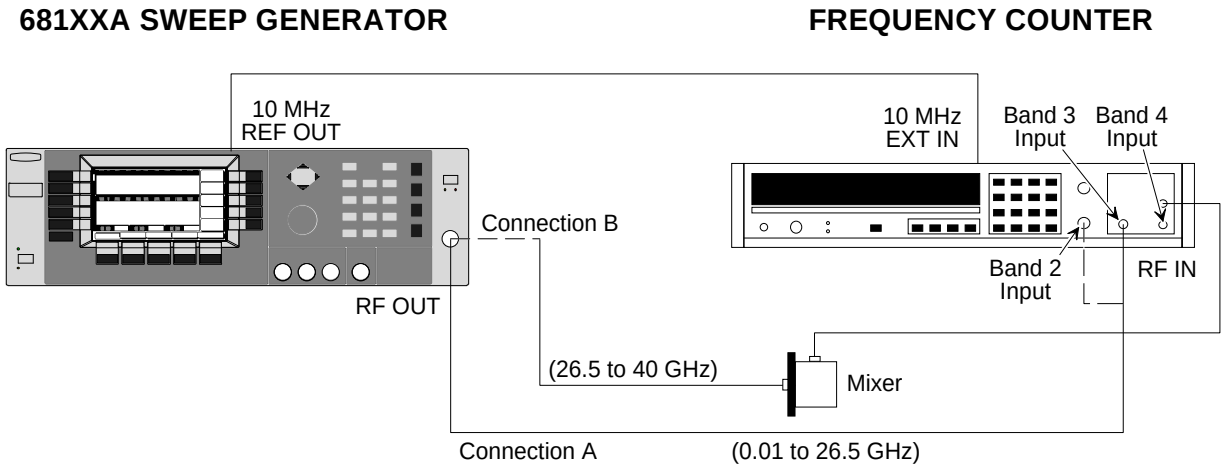


Figure 3-2. *Equipment Setup for Frequency Synthesis Tests*

Test Setup

Connect the equipment, shown in Figure 3-2, as follows:

1. Connect the 681XXA rear panel 10 MHz REF OUT to the Frequency Counter 10 MHz External Reference input. If the Frequency Counter has an INT/EXT toggle switch, ensure the switch is set to EXT.

2. Connect the 681XXA RF OUTPUT to the Frequency Counter RF Input as follows:
   a. For measuring frequencies of 0.01 to 1.0 GHz, connect to the Band 2 input (Connection A).
   b. For measuring frequencies of 1.0 to 26.5 GHz, connect to the Band 3 input (Connection A).
   c. For measuring frequencies of 26.5 to 40.0 GHz, connect to the Band 4 input via the Option 91 waveguide mixer (Connection B).

Coarse Loop/ YIG Loop Test Procedure

The following procedure tests both the coarse loop and YIG loop by stepping the sweep generator through its full frequency range in 1 GHz steps and measuring the RF output at each step.

1. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset, the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to the first test frequency indicated on the Test Record for the model being tested.

2. Record the Frequency Counter reading on the Test Record. The Frequency Counter reading must be within ±100 Hz of the displayed 681XXA frequency to accurately complete this test.

   NOTE

   The Frequency Counter reading is typically within ±1 Hz because the instruments use a common time base. Differences of a few Hertz can be caused by noise or counter limitations. Differences of ≥±100 Hz indicate a frequency synthesis problem.

3. On the 681XXA, use the cursor control key (diamond-shaped key) to increment F1 to the next test frequency on the Test Record. Record the Frequency Counter reading on the Test Record.

4. Repeat step 3 until all frequencies listed on the Test Record have been recorded.

Fine Loop Test Procedure

The following procedure tests the fine loop by stepping the instrument through ten 1 kHz steps (ten 100 Hz steps for instruments with Option 11) and measuring the RF output at each step.

1. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset, the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to the first test frequency indicated on the Test Record.

2. Record the Frequency Counter reading on the Test Record. The Frequency Counter reading must be within ±100 Hz of the displayed 681XXA frequency (±10 Hz for instruments with Option 11) to accurately complete this test.

3. On the 681XXA, use the cursor control key (diamond-shaped key) to increment F1 to the next test frequency on the Test Record. Record the Frequency Counter reading on the Test Record.

4. Repeat step 3 until all frequencies listed on the Test Record have been recorded.

3-7 SPURIOUS SIGNALS TEST: RF OUTPUT SIGNALS ≤2 GHz

The following test can be used to verify that the sweep generator meets its 0.01 to 2 GHz spurious signals (harmonic and non-harmonic) specifications. This test is applicable only to the 68147A and 68169A models.

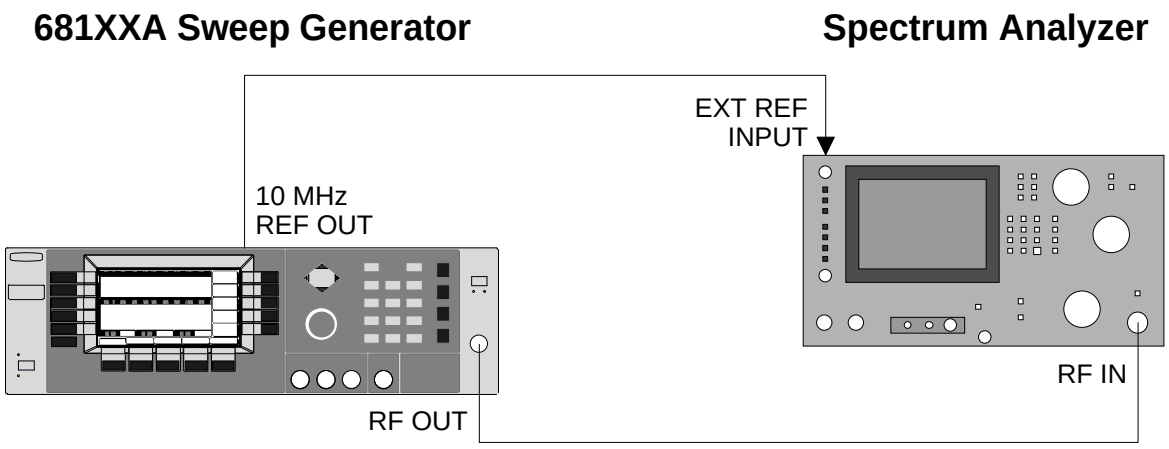


Figure 3-3. *Equipment Setup for Spurious Signals Test: RF Output Signals≤2 GHz*

Test Setup

Connect the equipment, shown in Figure 3-3, as follows:

1. Connect the 681XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.
2. Connect the 681XXA RF OUTPUT to the Spectrum Analyzer RF Input.

Test Procedure

The following procedure lets you measure the worst case spurious signals (harmonic and non-harmonic) of the 0.01 to 2 GHz RF output to verify that they meet specifications.

1. Set up the Spectrum Analyzer as follows:
   a. Span: 10 MHz/div
   b. CF: 50 MHz
   c. RBW: 1 MHz
   d. Sweep Time/Div: Auto (to resolve signal peaks clearly)

Table 3-2. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68147A	+13 dBM	+10 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

Table 3-3. *Spurious Signals Specifications*

Harmonic and Harmonic Related (Models 68147A and 68169A):
- **10 MHz to 50 MHz:** <–30 dBc
- **>50 MHz to ≤2 GHz:** <–40 dBc
- **>2 GHz to ≤20 GHz:** <–60 GHz
- **>20 GHz to ≤40 GHz:** <–40 dBc

Harmonic and Harmonic Related (Model 68147A with Option 15):
- **10 MHz to 50 MHz:** <–30 dBc
- **>50 MHz to ≤2 GHz:** <–40 dBc
- **>2 GHz to ≤20 GHz:** <–50 dBc

Non-Harmonics:
- **10 MHz to ≤2 GHz:** <–40 dBc
- **>2 GHz to ≤40 GHz:** <–60 dBc

2. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit L1** to open the current power level parameter for editing.
   c. Set L1 to the lesser of +10 dBm or the maximum leveled power level for the instrument being tested (refer to Table 3-2).
   d. Press **Edit F1** to open the current frequency parameter for editing.
   e. Set F1 to 10 MHz.

3. On the Spectrum Analyzer, measure the worst case harmonic and non-harmonic signals for the 10 MHz carrier. Record their presence by entering the levels on the Test Record. Refer to Table 3-3 for the specified level limits.

NOTE

Harmonics appear at multiples of the CW frequency and diminish quickly as the CW frequency gets greater than 1 GHz.

4. Repeat step 3 with F1 set first to 20 MHz, then set to 30 MHz. Measure the worst case harmonics and non-harmonics for each carrier frequency and record their presence by entering their levels on the Test Record.

5. Change the Spectrum Analyzer setup as follows:
   a. Span: 100 MHz/div
   b. CF: 500 MHz

6. Repeat step 3 with F1 set to 40 MHz. Measure the worst case harmonic and non-harmonic signals for the 40 MHz carrier and record their presence by entering their levels on the Test Record.

7. Change the Spectrum Analyzer setup as follows:
   a. Span: 200 MHz/div (or maximum span width)
   b. CF: 1 GHz (N/A is at maximum span width)

8. Repeat step 3 with F1 set to 350 MHz. Measure the worst case harmonic and non-harmonic signals for the 350 MHz carrier and record their presence by entering their levels on the Test Record.

9. Set F1 to 1.6 GHz. Measure the worst case non-harmonic signal for the 1.6 GHz carrier and record its presence by entering its level on the Test Record.

10. Change the Spectrum Analyzer setup as follows:
    a. Span: 10 MHz/div
    b. CF: 1.6 GHz
    c. RBW: 1 MHz

11. Adjust the Spectrum Analyzer Reference Level control to place the signal at the top of the screen graticule.

12. Change the Spectrum Analyzer CF first to 3.2 GHz, then to 4.8 GHz. Compare the harmonic levels with the signal level at 1.6 GHz. Measure the harmonic levels and record them on the Test Record.

3-8 HARMONIC TEST: RF OUTPUT SIGNALS FROM 2 TO 20 GHz

The following test can be used to verify that the sweep generator meets its harmonic specifications for RF output signals from 2 to 20 GHz. Test record entries are supplied for harmonics up to a frequency limit of 40 GHz. Additional harmonic checks may be made at any frequency of interest up to the RF output frequency limit of the 681XXA model being tested. These additional harmonic checks can be accomplished through the use of waveguide mixers to extend the frequency range of the spectrum analyzer.

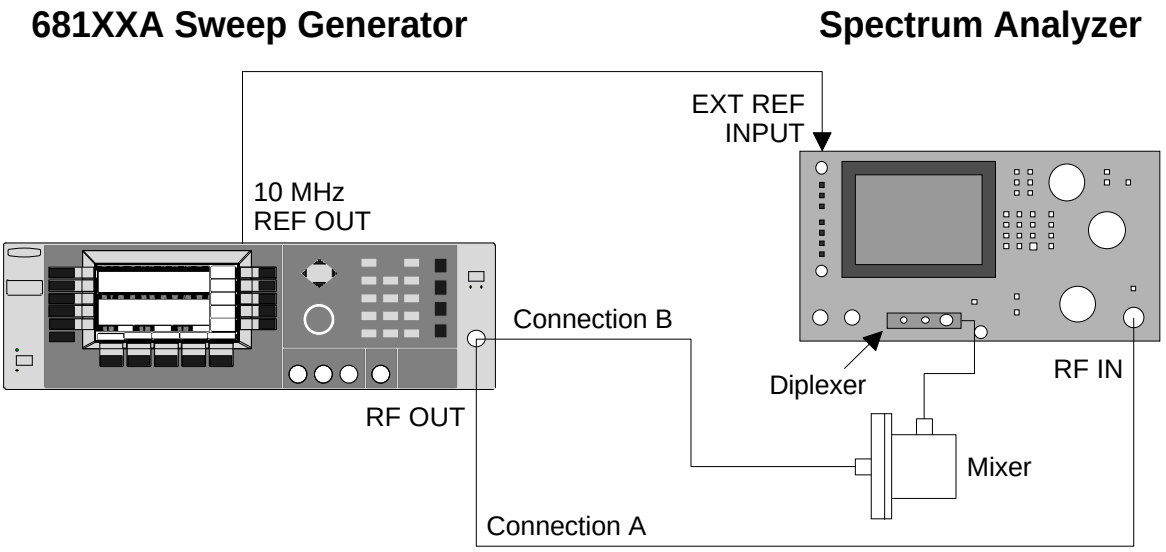


Figure 3-4. *Equipment Setup for Harmonic Test: RF Output Signals from 2 to 20 GHz*

Test Setup

Connect the equipment, shown in Figure 3-4, as follows:

1. Connect the 681XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.
2. Connect the diplexer and appropriate external waveguide mixer to the Spectrum Analyzer.
3. Connect the 681XXA RF OUTPUT to the Spectrum Analyzer as shown in Connection A (681XXA RF OUTPUT to Spectrum Analyzer RF IN).

Test Procedure (2 to 10 GHz)

The following procedure lets you measure the 2 to 10 GHz RF output harmonic levels to verify that they meet specifications.

1. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM**, then **Reset**. Upon reset the CW Menu is displayed.
   b. Press **Edit L1** to open the current power level parameter for editing.
   c. Set L1 to the lesser of +10 dBm or the maximum leveled power level for the instrument being tested (refer to Table 3-4).
   d. Press **Edit F1** to open the current frequency parameter for editing.
   e. Set F1 to the frequency indicated on the Test Record.
2. Set up the Spectrum Analyzer as follows:
   a. Span: 5 kHz/div
   b. CF: Set to the 681XXA frequency value.
   c. RBW: 1 kHz
   d. Video Filter Wide: On
3. Adjust the Spectrum Analyzer Peaking control for maximum signal level, then adjust the Reference Level Control to place the signal at the top of the screen graticule.
4. Change the Spectrum Analyzer CF to each of the harmonic frequencies listed on the Test Record and record the signal levels. Refer to Table 3-5 for the specified harmonic signal level limits.
5. Repeat steps 1 through 4 for each of the 681XXA CW carrier and harmonic frequencies listed on the Test Record. Record the harmonic signal levels on the Test Record.

Table 3-4. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68137A	+13 dBm	+10 dBm
68147A	+13 dBm	+10 dBm
68163A	+6 dBm	+2 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68137A	+17 dBm	+14 dBm
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

Table 3-5. *Spurious Signals Specifications*

Harmonic and Harmonic Related (Models 68137A, 68147A, 68163A, and 68169A):
>2 GHz to ≤20 GHz: <–60 dBc
>20 GHz to ≤40 GHz: <–40 dBc
Harmonic and Harmonic Related: (Models 68137A and 68147A with Option 15):
>2 GHz to ≤20 GHz: <–50 dBc
Non-Harmonics:
>2 GHz to ≤40 GHz: <–60 dBc

Test Procedure (11 to 20 GHz)

The following procedure lets you measure the 11 to 20 GHz RF output harmonic levels to verify that they meet specifications.

NOTE

Because an external mixer is required for these measurements, the RF output flatness of the 681XXA instrument is used to correct for; (1) variations caused by switching from the fundamental input to the external mixer input of the Spectrum Analyzer, and (2) the flatness of the mixer.

1. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to the frequency indicated on the Test Record.
   d. Press **Edit L1** to open the current power level parameter for editing.
   e. Set L1 to –30 dBm output power.

NOTE

If the 681XXA is not fitted with Option 2, install a 30 dB attenuator (Wiltron 41KC-20 and 41KC-10) and set L1 to 0.0 dBm output power.

2. Set up the Spectrum Analyzer as follows:
   a. Span: 5 kHz/div
   b. CF: Set to the 681XXA frequency value.
   c. RBW: 1 kHz
   d. Video Filter Wide: On

3. Adjust the Spectrum Analyzer Peaking control for maximum signal, then adjust the Reference Level control to place the signal at the top of the screen graticule. It may be necessary to also adjust the 681XXA output power level slightly to accomplish this; however, *do not exceed –-20 dBm output power*.

4. Remove Connection A and connect the 681XXA RF OUTPUT to the waveguide mixer input of the Spectrum Analyzer as shown in Connection B.

5. On the 681XXA, remove 30 dB of attenuation from the RF output. Do this by either increasing the output power level by 30 dB or by removing the 30 dB attenuator installed in step 1.e.

6. Change the Spectrum Analyzer CF to the harmonic frequency listed on the Test Record. Verify that the signal displayed on the Spectrum Analyzer is >10 dB below the top of the screen graticule.

NOTE

The <–10 dB signal level plus the 30 dB attenuation provided by the waveguide mixer equals a harmonic frequency signal level of <–40 dBc (specification).

7. Record the harmonic signal level on the Test Record.

8. Repeat steps 1 through 7 for each of the 681XXA CW carrier and harmonic frequencies listed on the Test Record. Record the harmonic signal levels on the Test Record.

3-9 SINGLE SIDEBAND PHASE NOISE TEST

The following test can be used to verify that the sweep generator meets its single sideband phase noise specifications. For this test, a second 681XXA is required. This additional sweep generator acts as a local oscillator (LO). The CW RF output of the 681XXA under test (DUT) is mixed with the CW RF output from the 681XXA LO which is offset by 1 MHz. Single sideband phase noise is measured at offsets of 100 Hz, 1 kHz, 10 kHz, and 100 kHz away from the resultant 1 MHz IF.

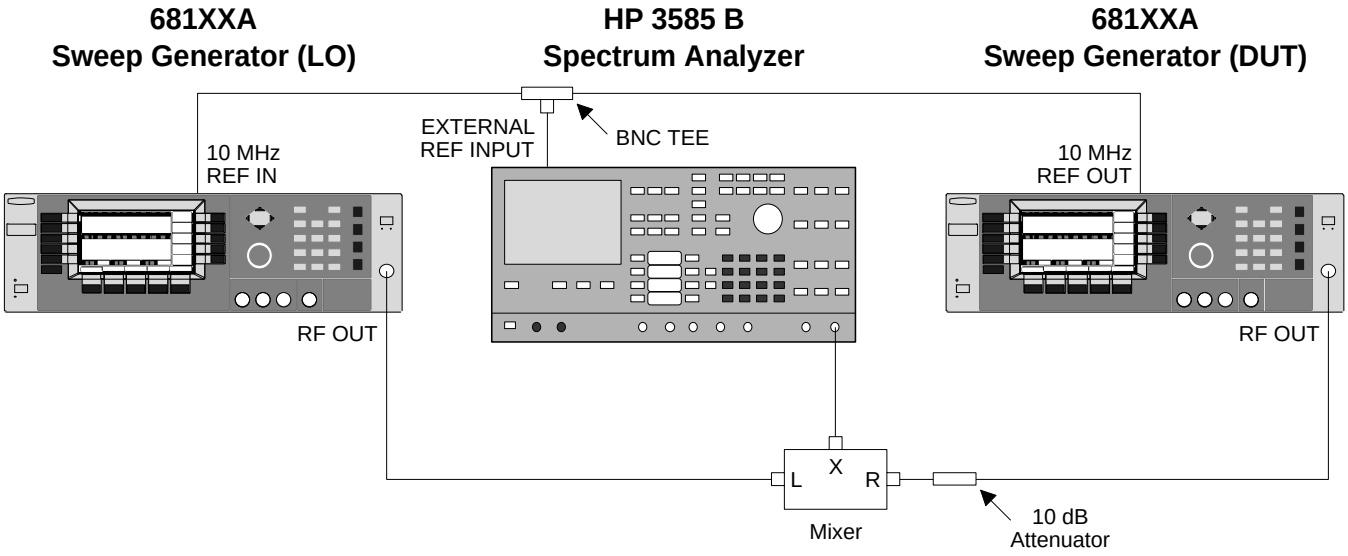


Figure 3-5. *Equipment Setup for Single Sideband Phase Noise Test*

Test Setup

Connect the equipment, shown in Figure 3-5, as follows:

1. Connect the 681XXA DUT rear panel 10 MHz REF OUT to the BNC tee. Connect one leg of the tee to the 681XXA LO rear panel 10 MHz REF IN. Connect the other leg of the tee to the Spectrum Analyzer External Reference Input.

2. Connect the 681XXA DUT RF OUTPUT to the Mixer's R input via a 10 dB attenuator.

3. Connect the 681XXA LO RF OUTPUT to the Mixer's L input.

4. Connect the Mixer's X output to the Spectrum Analyzer 50Ω input.

Test Procedure

The following procedure lets you measure the RF output single sideband phase noise levels to verify that they meet specifications.

NOTE

The following technique is a measurement of phase noise and AM noise. To avoid erroneous results, on the 681XXA DUT set L1 for maximum leveled output power and select External Detector leveling. This will prevent any AM noise from degrading the phase noise measurements.

1. Set up the 681XXA DUT as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to the frequency indicated on the Test Record.
   d. Press **Edit L1** to open the current power level parameter for editing.
   e. Set L1 to the maximum leveled power level for the instrument being tested (refer to Table 3-6).

2. Set up the 681XXA LO as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to a frequency that is 1 MHz lower than the 681XXA DUT frequency set in step 1.c.
   d. Press **Edit L1** to open the current power level parameter for editing.
   e. Set L1 to the maximum leveled power level for the instrument model (refer to Table 3-6).

NOTE

If the 681XXA LO output is less than 10 dBm, the Mixer's local oscillator port will not be saturated and the resulting measurements may be in error.

Table 3-6. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68137A	+13 dBm	+10 dBm
68147A	+13 dBm	+10 dBm
68163A	+6 dBm	+2 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68137A	+17 dBm	+14 dBm
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

Table 3-7. *Single Sideband Phase Noise Test Specification*

CW Carrier Frequency	Offset From Carrier	Test Specification*
0.01 to 8.4 GHz	100 Hz	<–67 dBc
	1 kHz	<–75 dBc
	10 kHz	<–83 dBc
	100 kHz	<–87 dBc
>8.4 to 20 GHz	100 Hz	<–58 dBc
	1 kHz	<–71 dBc
	10 kHz	<–73 dBc
	100 kHz	<–82 dBc
>20 to 40 GHz	100 Hz	<–52 dBc
	1 kHz	<–65 dBc
	10 kHz	<–67 dBc
	100 kHz	<–76 dBc

* 3 dB difference from 681XXA single sideband phase noise specifications to account for LO phase noise.

3. Set up the Spectrum Analyzer as follows:
   a. Center Frequency: 1 MHz
   b. Frequency Span: 300 Hz
   c. RBW: 3 Hz
   d. Position the Marker to the peak of the signal.
   e. Select OFFSET, ENTER OFFSET, and MKRCF.
   f. Adjust the marker for a 100 Hz offset.
   g. Select NOISE LVL.
4. Measure the phase noise level 100 Hz offset from the carrier frequency. Record the level on the Test Record.
5. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 20 kHz.
   c. Set RBW to 100 Hz.
   d. Adjust the Marker for a 1 kHz offset.
   e. Select NOISE LVL.
6. Measure the phase noise level 1 kHz offset from the carrier frequency. Record the level on the Test Record.
7. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 100 kHz.
   c. Adjust the Marker for a 10 kHz offset.
   d. Select NOISE LVL.
8. Measure the phase noise level 10 kHz offset from the carrier frequency. Record the level on the Test Record.

9. On the Spectrum Analyzer:
   a. Deselect NOISE LVL.
   b. Set Frequency Span to 300 kHz.
   c. Adjust the Marker for a 100 kHz offset.
   d. Select NOISE LVL.
10. Measure the phase noise level 100 kHz offset from the carrier frequency. Record the level on the Test Record.
11. Repeat steps 1 through 10 for all frequencies listed on the Test Record.

3-10 POWER LEVEL ACCURACY AND FLATNESS TESTS

The following tests can be used to verify that the 681XXA meets its power level specifications. Power level verification testing is divided into two parts—power level accuracy tests and power level flatness tests.

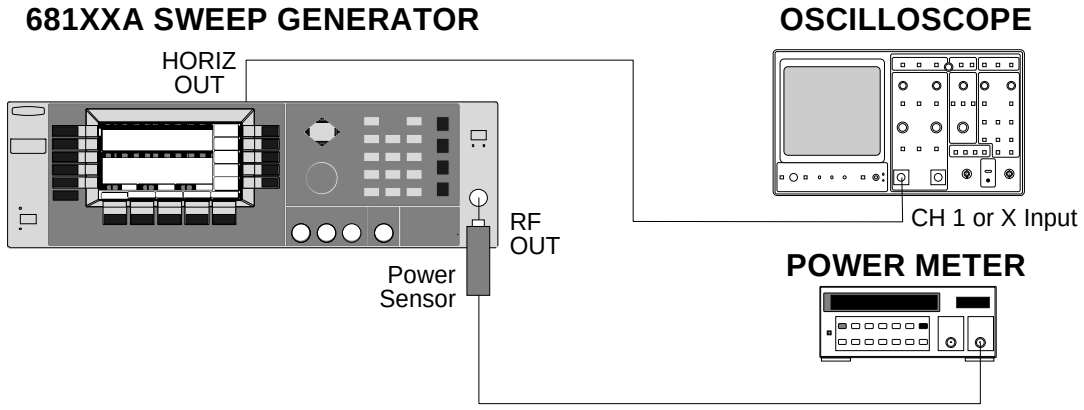


Figure 3-6. *Equipment Setup for Power Level Accuracy and Flatness Tests*

Test Setup

Connect the equipment, shown in Figure 3-6, as follows:

1. Calibrate the Power Meter with the Power Sensor.
2. Using the K (male) to 2.4 mm (female) adapter, connect the Power Sensor to the RF OUTPUT of the 681XXA.
3. Connect the 681XXA rear panel HORIZ OUT to the Oscilloscope CH.1 input (X input).

NOTE

During this test it will be necessary to adjust the Power Meter's CAL FACTOR % setting as applicable for the frequency being tested.

Power Level Accuracy Test Procedure

The following procedure tests power level accuracy by stepping the output power level down in 1 dB increments from its maximum rated power level and measuring the output power level at each step.

1. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset, the CW Menu is displayed.
   b. Press **Edit F1** to open the current frequency parameter for editing.
   c. Set F1 to the CW frequency indicated on the Test Record.
   d. Press **Edit L1** to open the current power level parameter for editing.
   e. Set L1 to the power level indicated on the Test Record.
2. Measure the output power level with the Power Meter and record the reading on the Test Record.
3. On the 681XXA, use the cursor control key (diamond-shaped key) to decrement L1 to the next test power level on the Test Record. Measure and record the Power Meter reading on the Test Record.
4. Repeat step 3 for each of the test power levels listed on the Test Record for the current CW frequency.
5. Repeat steps 1 thru 4 for all CW frequencies listed on the Test Record.

Power Level Flatness Test Procedure

The following procedure tests power level flatness by measuring the output power level variation during a full band sweep; first in the step sweep mode, then in the analog sweep mode.

1. Set up the 681XXA as follows for a step sweep power level flatness test:
   a. Reset the instrument by pressing **SYSTEM**, then **Reset**. The CW Menu is displayed.
   b. Press **Step** to place the 681XXA in the step sweep frequency mode and display the Step Sweep Menu.
   c. With the Step Sweep Menu displayed, press the main menu key

      FREQUENCY CONTROL

      The Sweep Frequency Control Menu is then displayed.
   d. Press **Full** to select a full range frequency sweep.
   e. Press **Edit L1** to open the current power level parameter for editing.
   f. Set L1 to the power level indicated on the test record.
   g. Now, return to the Step Sweep Menu by pressing the main menu key

      CW/SWEEP SELECT
   h. At the Step Sweep Menu, press **Sweep Ramp** to go to the Step Sweep Ramp Menu.
   i. At this menu, press **Dwell Time** to open the dwell time-per-step parameter for editing.
   j. Set the dwell time to 1 second.

      NOTE
      Monitor the 681XXA's Horizontal Output on the Oscilloscope to determine sweep start and stop.

2. As the 681XXA steps through the full frequency range, measure the maximum and minimum Power Meter readings and record the values on the Test Record. Verify that the variation (difference between the maximum and minimum readings) does not exceed the value noted on the Test Record.

3. Set up the 681XXA as follows for an analog sweep power level flatness test:
   a. Reset the instrument by pressing **SYSTEM**, then **Reset** . The CW Menu is displayed.
   b. Press **Analog** to place the 681XXA in the analog sweep frequency mode and display the Analog Sweep Menu.
   c. With the Analog Sweep Menu displayed, press the main menu key

      FREQUENCY CONTROL

      The Sweep Frequency Control Menu is then displayed.
   d. Press **Full** to select a full range frequency sweep.
   e. Press **Edit L1** to open the current power level parameter for editing.
   f. Set L1 to the power level noted on the test record.
   g. Now, return to the Analog Sweep Menu by pressing the main menu key

      CW/SWEEP SELECT
   h. At the Analog Sweep Menu, press the menu soft-key **Sweep Ramp** to go to the Analog Sweep Ramp Menu.
   i. At this menu, press **Sweep Time** to open the sweep time parameter for editing.
   j. Set the sweep time to 99 seconds.

      NOTE
      Monitor the 681XXA's Horizontal Output on the Oscilloscope to determine sweep start and stop.

4. During the analog sweep, measure the maximum and minimum Power Meter readings and record the values on the Test Record. Verify that the variation (difference between the maximum and minimum readings) does not exceed the value noted on the Test Record.

Chapter 4
Calibration

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Chapter 4
Calibration

4-1 INTRODUCTION

This chapter contains procedures for calibrating the Series 681XXA Synthesized Sweep Generator. These procedures are typically accomplished because out-of-tolerance conditions have been noted during performance verification testing (see Chapter 3) or as a result of replacement of subassemblies or RF components.

NOTE

The calibration procedures herein support operating firmware Version 1.15 and above. It is recommended that you upgrade your instrument's operating firmware to the latest available version prior to calibration. For assistance in calibrating instruments containing older versions of the operating firmware or for firmware upgrade details, contact your local WILTRON service center.

4-2 RECOMMENDED TEST EQUIPMENT

Table 4-1 (page 4-5) provides a list of the recommended test equipment for these calibration procedures.

The procedures refer to specific test equipment front panel control settings when the test setup is critical to making accurate measurements. In some cases, the user may substitute test equipment having the same critical specifications as those on the recommended test equipment list.

Contact your local WILTRON service center (Refer to Table 1-5 on page 1-15) if you need clarification of any equipment or procedural reference.

4-3 TEST RECORDS

A blank copy of a sample calibration test record for each 681XXA model is provided in Appendix A. Each test record contains model-specific variables called for by the calibration procedures. It also provides a means for maintaining an accurate and complete record of instrument calibration. We recommend that you copy these pages and use them to record the results from (1) your initial calibration of out-of-tolerance 681XXA circuits, or (2) your initial calibration of the 681XXA following replacement of subassemblies or RF components. These initial readings can be used later as benchmark values for future tests of the same serial-numbered instruments.

4-4 CALIBRATION FOLLOWING SUBASSEMBLY REPLACEMENT

Table 4-2 (page 4-6) lists the calibration that should be performed following the replacement of 681XXA subassemblies or RF components.

4-5 CONNECTOR AND KEY LABEL NOTATION

The calibration procedures include many references to equipment interconnections and control settings. For all 681XXA references, specific labels are used to denote the appropriate menu key, data entry key, data entry control, or connector (such as CW/SWEEP SELECT or RF OUTPUT). Most references to supporting test equipment use general labels for commonly used controls and connections (such as Span or RF Input). In some cases, a specific label is used that is a particular feature of the test equipment listed in Table 4-1.

Table 4-1. *Recommended Test Equipment for Calibration Procedures*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	PROCEDURE NUMBER
Frequency Counter	*Frequency Range:* 1 to 18 GHz *Input Impedance:* 50Ω *Resolution:* 1 Hz	EIP Microwave, Inc. Model 578A	4-7
Spectrum Analyzer	*Frequency Range:* 1 to 5 GHz *Resolution Bandwidth:* 10 Hz	Tektronix, Model 2794	4-12, 4-13
Spectrum Analyzer	*Frequency Range:* 20 Hz to 40 MHz *Resolution Bandwidth:* ≤3 MHz	Hewlett-Packard, Model 3585B	4-11
Digital Multimeter	*Resolution:* 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% +2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% +100 counts (to 20 kHz) *AC Input Impedance:* 10 MΩ	John Fluke, Inc., Model 8840A, with Option 8840A-09 (True RMS AC)	4-12, 4-13
Function Generator	*Output Voltage:* 1 volt peak-to-peak *Functions:* 0.5 Hz to 100 kHz sine and square waveforms	Hewlett-Packard, Model 8116A	4-12, 4-13
Modulation Analyzer	*Frequency Input:* 10 MHz (or the IF of the Spectrum Analyzer) *AM Depth:* 0% to 90% *AM Modulation Rates:* DC to 100 kHz *Filters:* 50 Hz lowpass, 15 kHz highpass	Hewlett-Packard, Model 8902A	4-12
Scalar Network Analyzer, with RF Detector	*Frequency Range:* 0.01 to 40 GHz	WILTRON Model 562, with RF Detector: 560-7K50 (0.01 to 40 GHz)	4-8, 4-9
Attenuator	*Frequency Range:* DC to 40 GHz *Max Input Power:* >+17 dBm *Attenuation:* 10 dB	WILTRON, Model 41KC-10	4-4-8, 4-9
RF Detector	*Frequency Range:* 0.01 to 40 GHz *Output Polarity:* Negative	WILTRON, Model 75KC50 (K input/BNC output connectors)	4-11
Personal Computer	*PC Configuration:* IBM AT or compatible *Operating System:* Windows 3.1 *Accessories:* Mouse	Any common source	All procedures
Serial Interface Assy	Provides serial interface between the PC and the 681XXA.	WILTRON P/N: T1678	All procedures
Tee	*Connectors:* 50Ω BNC	Any common source	4-12, 4-13
Cables	*Connectors:* 50Ω BNC	Any common source	All procedures

Table 4-2. *Calibration Following Subassembly/RF Component Replacement*

Subassembly/RF Component Replaced	Perform the Following Calibration(s) in Paragraph(s):
A1, A2 Front Panel Assy	None
A3 Reference Loop PCB	4-7
A4 Coarse Loop PCB	4-7
A5 Fine Loop PCB	4-7
A6 Square Wave Generator PCB	None
A7 YIG Loop PCB	None
A9 PIN Control PCB	4-8, 4-9, 4-10, 4-11
A9-1 PIN Control PCB	4-8, 4-9, 4-10, 4-11
A10 ALC PCB	4-8, 4-9, 4-10, 4-11, 4-12
A11 AM/FM PCB	4-7, 4-13
A12 Analog Instruction PCB	4-7
A13 YIG Driver PCB	4-7
A14 Doubler Driver PCB	4-8
A14-1 SDM Driver PCB	None
A15 Regulator PCB	None
A16 CPU Interface PCB	None
A17 CPU PCB	4-8 thru 4-13. None, if firmware EEPROMs are reused.
A18 Power Supply PCB	None
A19 AC Line Conditioner PCB	None
A21 Line Filter/Rectifier PCB	None
A21-1 BNC/GPIB Connector PCB	None
YIG-tuned Oscillator	4-7
0.01 to 2 GHz Down Converter Assy	4-8, 4-9, 4-10, 4-11
Switched Filter Assy	4-8, 4-9, 4-10, 4-11
Frequency Extension Unit (FEU)	4-7, 4-8, 4-9, 4-10, 4-11
Switched Doubler Module (SDM)	4-8, 4-9, 4-10, 4-11
Directional Coupler	4-8, 4-9, 4-10, 4-11
Step Attenuator	4-8, 4-9, 4-10

4-6 INITIAL SETUP

The 681XXA is calibrated using an IBM compatible PC and external test equipment. The PC must have the Windows operating system, Version 3.1, installed and be equipped with a mouse. Initial setup consists of interfacing the PC to the sweep generator.

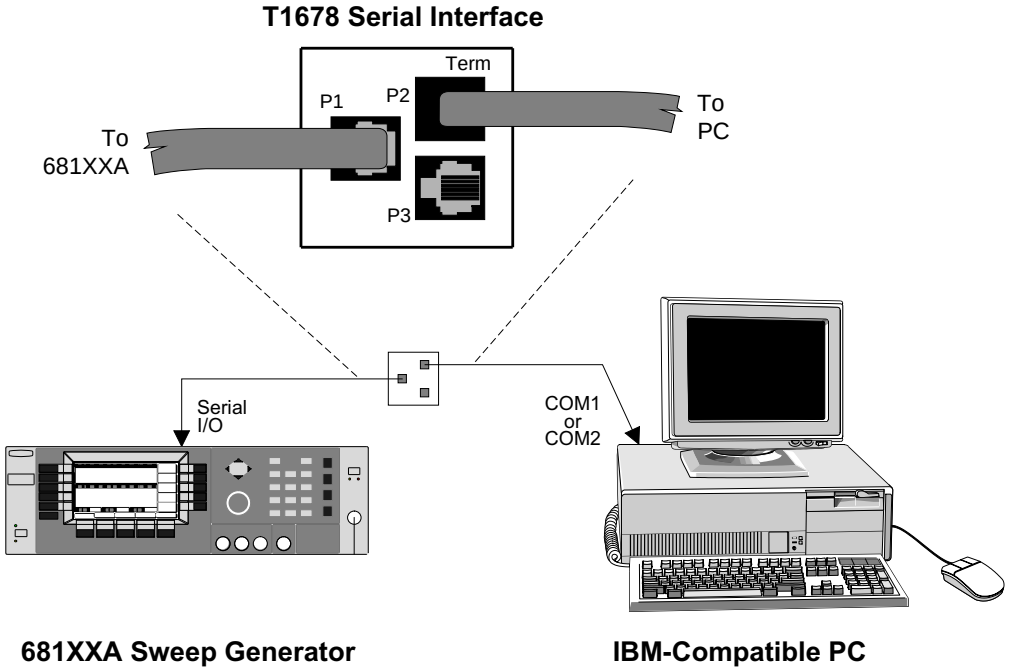


Figure 4-1. *PC to 681XXA Interconnection for Calibration*

Interconnection

Using the WILTRON P/N T1678 serial interface assembly, connect the PC to the 681XXA as follows:

1. Connect the wide flat cable between the 681XXA rear panel SERIAL I/O connector and the P1 connector on the T1678 serial interface PCB.

2. Connect the narrow flat cable between the P2 (TERM) connector on the T1678 serial interface PCB and the COM1 or COM2 connector on the PC. Use the RJ11-to-DB-9 or RJ11-to-DB-25 adapter, provided with the T1678 serial interface assembly, to make the connection at the PC.

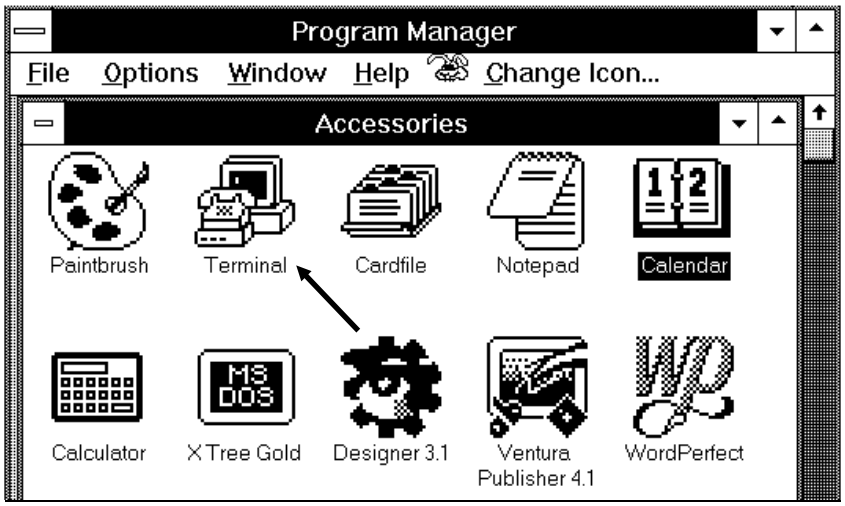
Configuring the PC

Configure the PC to interface with the 681XXA as follows:

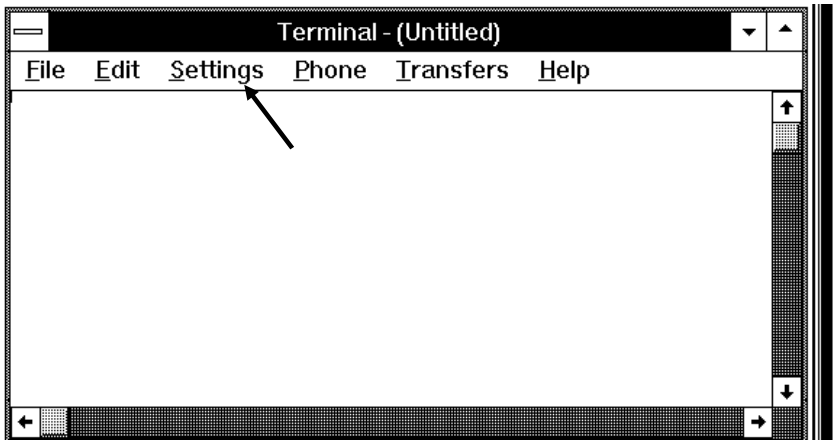
1. Power up the 681XXA.

2. Power up the PC and place in Windows.

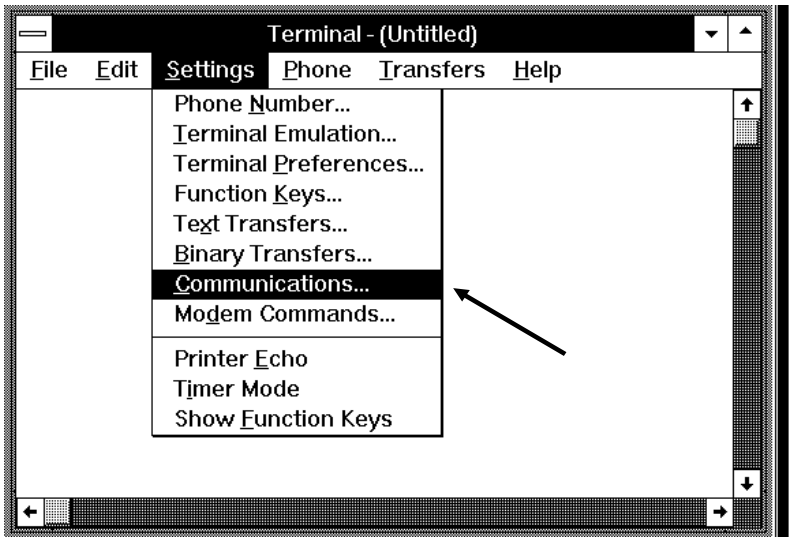
3. Double click on the Terminal Icon to bring up the Terminal (Untitled) window. The initial installation of Windows places the Terminal Icon in the Accessories window.



4. At the Terminal window, click on Settings to display the Settings menu.

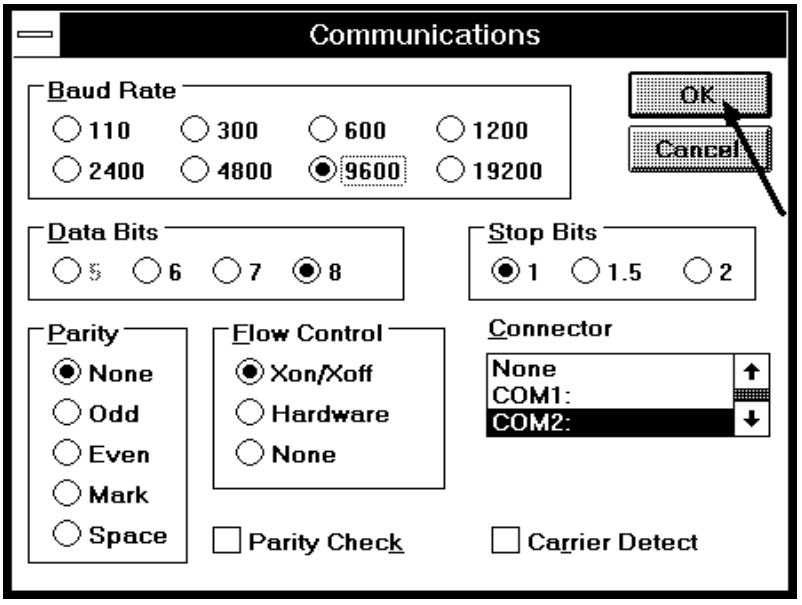


5. Click on Communications.



6. At the Communications Dialog box, select the following options:

Baud Rate	9600
Data Bits	8
Stop Bits	1
Parity	None
Flow Control	Xon/Xoff
Connector	Select connection made during interconnection



7. After making the selections, click on the OK button.

8. Press <ENTER> on the keyboard.

9. Verify that a **$** prompt appears on the PC display.

10. This completes the initial setup for calibration.

4-7 PRELIMINARY CALIBRATION

This procedure provides the steps necessary to initially calibrate the coarse loop, fine loop, frequency instruction, and internal DVM circuitry and the 100 MHz reference oscillator of the 681XXA sweep generator.

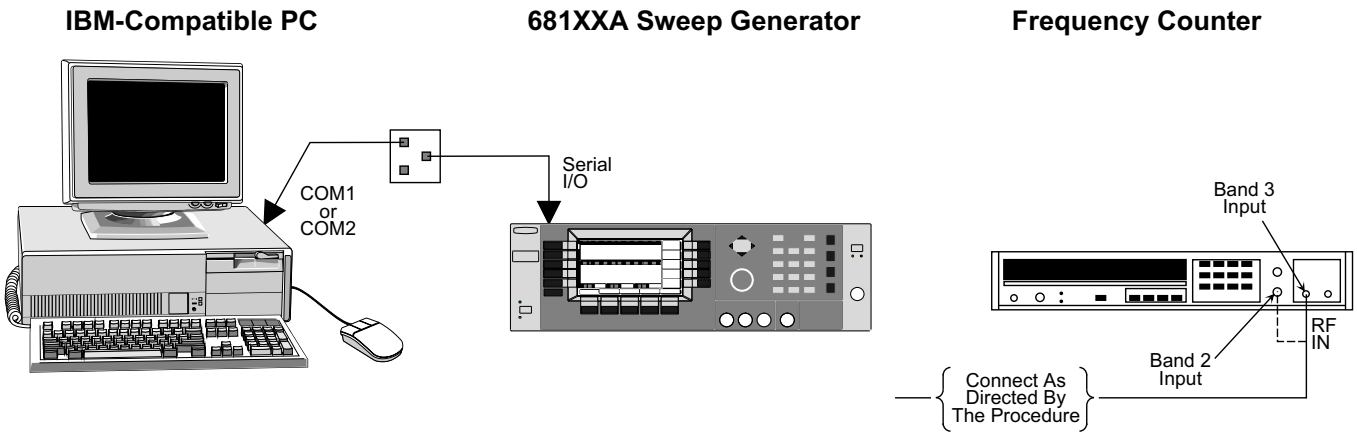


Figure 4-2. *Equipment Setup for Preliminary Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-2, as follows:

1. Interface the PC to the 681XXA by performing the initial setup procedure, pages 4-7 to 4-10.

2. Connect the Frequency Counter to the 681XXA when directed to do so during the calibration procedure.

NOTE

Before beginning this calibration procedure, *always* let the 681XXA warm up for a minimum of one hour.

Resetting the Linearizer DACs

Before actual calibration of the 681XXA can begin, the 2 to 8.4 GHz and 8.4 to 20 GHz settings of the YIG Frequency Linearizer DACs must first be reset.

1. Reset the Linearizer DACs as follows:
   a. At the **$** prompt, type: **drct_cal** and press <ENTER>. A menu of items and their values is displayed on the screen.
   b. Select Items 40 and 41 from the menu and set their values to 0 by following the instructions presented at the bottom of the screen.
   c. Follow the instructions presented to exit the program.

2. Store the new DAC values as follows:
   a. At the **$** prompt, type the following:

      send 3 303 and press <ENTER>
      cal_code & and press <ENTER>
      calterm 787 and press <ENTER>

      The **$** prompt will appear on the screen when the data has been stored.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

Calibration Steps

Each of the steps in this procedure provides initial calibration of a specific 681XXA circuit or component. To ensure accurate instrument calibration, each step of this procedure must be performed in sequence.

1. Calibrate the internal DVM circuitry as follows:
   a. At the **$** prompt, type: **calterm 119** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

2. Calibrate the Coarse Loop Pretune DAC as follows:
   a. At the **$** prompt, type: **calterm 137** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

NOTE

To save the calibration data after completing any calibration step, type: **calterm 787** and press <ENTER>.

3. Calibrate the Fine Loop Pretune DAC as follows:
   a. At the **$** prompt, type: **calterm 136** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

4. Calibrate the Sweep Time DAC as follows:
   a. At the **$** prompt, type: **calterm 132** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

5. Calibrate the Center Frequency DAC as follows:
   a. At the **$** prompt, type: **calterm 114** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

6. Calibrate the YIG Frequency Offset DAC as follows:
   a. At the **$** prompt, type: **calterm 134** and press <ENTER>.
   b. Follow the instructions on the screen.

NOTE

Adjust the DAC to the number that will get the closest to the 100 MHz below 2 GHz and 100 MHz below 8.4 GHz called for by the procedure.

   c. Record step completion on the Test Record.

7. Calibrate the YIG Frequency Linearizer DACs as follows:
   a. At the **$** prompt, type: **calterm 127** and press <ENTER>.
   b. Follow the instructions on the screen and enter the value of the frequency counter reading at approximately 2 GHz.
   c. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, or 0 to decrement the 681XXA's frequency. Set the frequency of the 681XXA to 6.000 GHz.
   d. Subtract 10 MHz from the frequency counter reading and enter this value. (*Example:* Frequency counter reading of 8118 – 10 MHz = 8108)
   e. Using the keyboard, as described in step 8.c, set the frequency of the 681XXA to 16.000 GHz.
   f. Record step completion on the Test Record.

8. Calibrate the 100 MHz Reference Oscillator as follows:
   a. If Option 16 (High Stability Time Base) is installed, disconnect the cable at A3J6.
   b. Connect the frequency counter to A3J3.
   c. At the **$** prompt, type: **calterm 130** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   d. Reconnect the cable to A3J6, if removed.
   e. Record step completion on the Test Record.

9. Calibrate the FM Coil Sensitivity Calibration DAC as follows:
   a. At the **$** prompt, type: **calterm 135** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration is complete.)
   b. Record step completion on the Test Record.

10. Calibrate the Sweep Width DAC as follows:
    a. At the **$** prompt, type: **calterm 133** and press <ENTER>. (This calibration can take approximately 2 minutes to complete.)

       The **$** prompt will appear on the screen when the calibration is complete.

    b. Record step completion on the Test Record.

NOTE

The following step is only required for instruments containing a FEU (Models 68163A and 68169A having serial numbers below 320001).

11. Calibrate the input power levels to the FEU as follows:
    a. At the **$** prompt, type: **calterm 140** and press <ENTER>.

    b. Enter the values for the FEU input power levels of +16 dBm and +18.5 dBm. The values are printed on the FEU label.

    c. Record step completion on the Test Record.

12. Store the calibration data as follows:
    a. At the **$** prompt, type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)

13. At the **$** prompt, type: **calterm 875** and press <ENTER> to exit the calibration program.

14. Turn the 681XXA off, then back on to return the instrument to normal operation.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-8 SWITCHED FILTER SHAPER CALIBRATION

This procedure provides the steps necessary to adjust the Switched Filter Shaper Amplifier gain to produce a more constant level amplifier gain with power level changes.

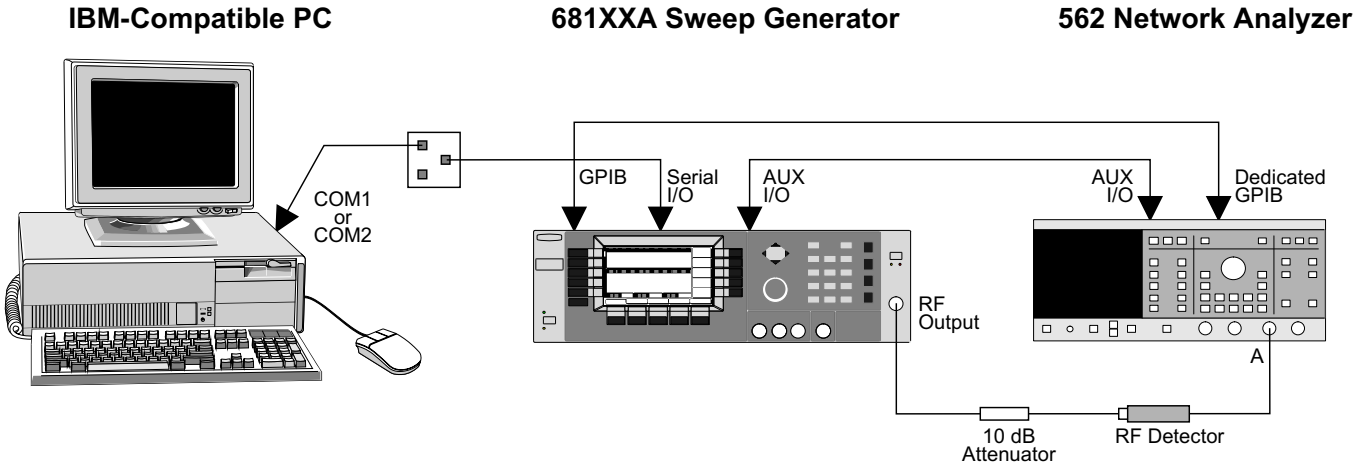


Figure 4-3. *Equipment Setup for Switched Filter Shaper Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-3, as follows:

1. Interface the PC to the 681XXA by performing the initial setup procedure, pages 4-7 to 4-10.

2. Using the Auxiliary I/O cable, connect the 681XXA rear panel AUX I/O connector to the 562 Network Analyzer AUX I/O connector.

3. Using the GPIB cable, connect the 562 Network Analyzer DEDICATED GPIB connector to the 681XXA IEEE-488 GPIB connector.

4. Connect the RF Detector to the 562 Network Analyzer Channel A Input connector.

5. Connect the 681XXA RF OUTPUT connector to the RF Detector via a 10 dB Attenuator.

NOTE

Before beginning this calibration procedure, *always* let the 681XXA warm up for a minimum of one hour.

Minimum Unleveled Power Point Measurement

Before the Switched Filter Shaper Amplifier can be adjusted, the frequency at which the minimum unleveled power point in each frequency band occurs must be determined.

1. Set up the 562 Network Analyzer as follows:
   a. Press the System Menu key.
   b. From the System Menu display, select RESET.
   c. Press CHANNEL 2 DISPLAY: OFF
   d. Press CHANNEL 1 DISPLAY: ON
   e. Press CHANNEL 1 MENU key.
   f. From the Channel 1 Menu display, select POWER.

2. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Analog** to select analog sweep mode.
   c. Press **FREQUENCY CONTROL** to display the Frequency Control Menu.

3. On the 681XXA:
   a. Press **Edit F1** and set F1 to the start frequency of the first frequency band shown on the Test Record.
   b. Press **Edit F2** and set F2 to the stop frequency of the first frequency band shown on the Test Record.
   c. Press **Edit L1** and increase the power level until either an unleveled condition occurs or the power level reaches maximum.

4. On the 562 Network Analyzer:
   a. Press CURSOR ON/OFF to turn the cursor on.
   b. Use the cursor to locate the minimum unleveled power point in the frequency range.

5. Record the frequency of the minimum unleveled power point on the Test Record.

6. Repeat steps 3 thru 5 for each frequency band listed on the Test Record.

Shaper DAC Adjustment

The following procedure lets you adjust the Switched Filter Shaper DAC which controls the gain of the Switched Filter Shaper Amplifier.

1. On the 562 Network Analyzer:
   a. Press SYSTEM MENU.
   b. On the System Menu display, highlight SYSTEM INTERFACE, then press SELECT.
   c. On the System Interface Menu display, highlight OFF, then press SELECT.

2. On the 681XXA:
   a. Press **CW/SWEEP SELECT** . The CW Menu is displayed.
   b. Press **Edit F1** and set F1 to the first minimum unleveled power point frequency recorded on the Test Record.
   c. Press **Edit L1** and set L1 to the maximum leveled power level for the instrument being calibrated (refer to Table 4-3).
   d. Press **LEVEL/ALC SELECT** . At the resulting menu display, press **ALC Mode** . The ALC Mode Menu is displayed.
   e. Press **Leveling Menu** to go to the Leveling Menu display, then press **Fixed Gain** to select the fixed gain leveling mode.
   f. Press **Lvl Sweep** . At the resulting CW Level Sweep Menu, press **Sweep Ramp** to display the CW Level Sweep Ramp Menu.
   g. Press **Dwell Time** and set the dwell time to 5 mS.
   h. Press **Num of Steps** and set the number of steps to 200.
   i. Press **Previous Menu** to return to the CW Level Sweep Menu display.
   j. Using the **Edit L1** and **Edit L2** keys and the data entry keys and controls, edit the values of L1 and L2 to produce a display on the 562 Network Analyzer similar to the one shown in Figure 4-4.

NOTE

The 681XXA is in fixed gain mode, therefore L1 and L2 do not represent actual power levels.

Table 4-3. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68137A	+13 dBm	+10 dBm
68147A	+13 dBm	+10 dBm
68163A	+6 dBm	+2 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68137A	+17 dBm	+14 dBm
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

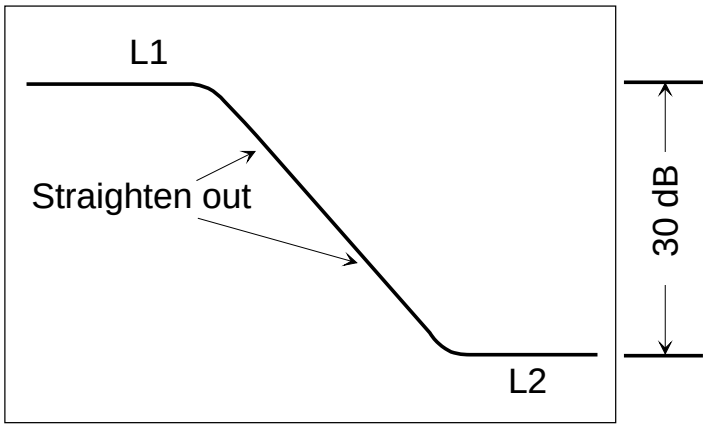


Figure 4-4. *Typical Switched Filter Shaper Calibration Waveform*

3. On the 562 Network Analyzer:
   a. Press OFFSET/RESOLUTION.
   b. Set Resolution to 5 dB/Div
   c. Adjust Offset to center the display.

4. Adjust the Switched Filter Shaper DAC for frequency bands between 0.01 and 20 GHz as follows:
   a. At the **$** prompt on the PC display, type: **`easy 25 128 8`** and press <ENTER>.
   b. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, or 0 to decrement the value of the DAC's setting to "straighten" the waveform being displayed on the 562 Network Analyzer.
   c. Record the DAC's setting value on the Test Record.

5. On the 681XXA:
   a. Press **CW/SWEEP SELECT** . At the resulting menu display, press **CW** . The CW Menu is displayed.
   b. Press **Edit F1** and set F1 to the frequency band start frequency + 100 MHz.
   c. Increment F1 in 100 MHz steps from the start frequency + 100 MHz to the stop frequency – 100 MHz of the frequency band and verify that no readjustment of the DAC is required.

6. Repeat steps 2 thru 5 for each frequency band listed on the Test Record.

7. Exit the program by pressing **Q** on the keyboard.

NOTE

The following procedure applies only to instruments with frequency ranges to 40 GHz and containing FEUs (Models 68163A and 68169A having serial numbers below 320001).

8. Perform steps 3 and 4 with F1 set to the minimum unleveled power point frequency recorded on the Test Record for the 20 to 26.5 GHz frequency band.

9. Adjust the Switched Filter Shaper DAC for frequency bands between 20 and 40 GHz as follows:
   a. At the **$** prompt on the PC display, type: **`easy 74 128 8`** and press <ENTER>.
   b. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, or 0 to decrement the value of the DAC's setting to "straighten" the waveform being displayed on the 562 Network Analyzer.
   c. Record the DAC's setting value on the Test Record.

10. On the 681XXA:
    a. Press **CW/SWEEP SELECT** . At the resulting menu display, press **CW** . The CW Menu is displayed.
    b. Press **Edit F1** and set F1 to the frequency band start frequency + 100 MHz.
    c. Increment F1 in 100 MHz steps from the start frequency + 100 MHz to the stop frequency – 100 MHz of the frequency band and verify that no readjustment of the DAC is required.

11. Repeat steps 2, 3, 9, and 10 for the 26.5 to 33 GHz and 33 to 40 GHz frequency bands.

12. Exit the program by pressing **Q** on the keyboard.

Entering DAC Settings

The following procedure provides steps for entering the new DAC setting values into RAM located on the A17 CPU PCB.

1. Enter the new DAC setting values as follows:
   a. At the **$** prompt, type: **drct_cal** and press <ENTER>. A menu is presented on the screen that lists all DACs and their current settings.

      The following items from the menu pertain to the Switched Filter Shaper DAC settings for the frequency bands listed:

Item 3	Band 0 (0.01-2.0 GHz)
Item 4	Band 1 (2.0 -3.3 GHz)
Item 5	Band 2 (3.3-5.5 GHz)
Item 6	Band 3 (5.5-8.4 GHz)
Item 7	Band 4 (8.4-13.25 GHz)
Item 8	Band 5 (13.25-20.0 GHz)
Item 9	Band 6 (20-26.5 GHz)
Item 10	Band 7 (26.5-33 GHz)
Item 11	Band 8 (33-40 GHz)

   b. Select the item that pertains to the Switched Filter Shaper DAC setting to be updated. Following the instructions presented on the bottom of the screen, enter the new DAC setting value from the Test Record.

   c. When you are finished entering all the new DAC setting values from the Test Record, exit the program.

Storing DAC Settings

The following procedure stores the new DAC setting values, entered above, in non-volatile memory (EEPROMs) located on the A17 CPU PCB.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

1. Store the new DAC setting values as follows:
   a. At the **$** prompt, type the following:

      send 3 303 and press <ENTER>
      cal_code & and press <ENTER>
      calterm 787 and press <ENTER>

      The **$** prompt will appear on the screen when the data has been stored.

2. At the **$** prompt, type: **calterm 875** and press <ENTER> to exit the calibration program.

3. Turn the 681XXA off, then back on to return the instrument to normal operation.

4-9 ALC SLOPE CALIBRATION

This procedure provides the steps necessary to perform ALC Slope calibration. The ALC Slope DAC is calibrated to adjust for an increasing or decreasing output power-vs-output frequency in the analog sweep mode. The ALC Slope DAC has two calibrations—one for frequencies ≤2 GHz and one for frequencies >2 GHz.

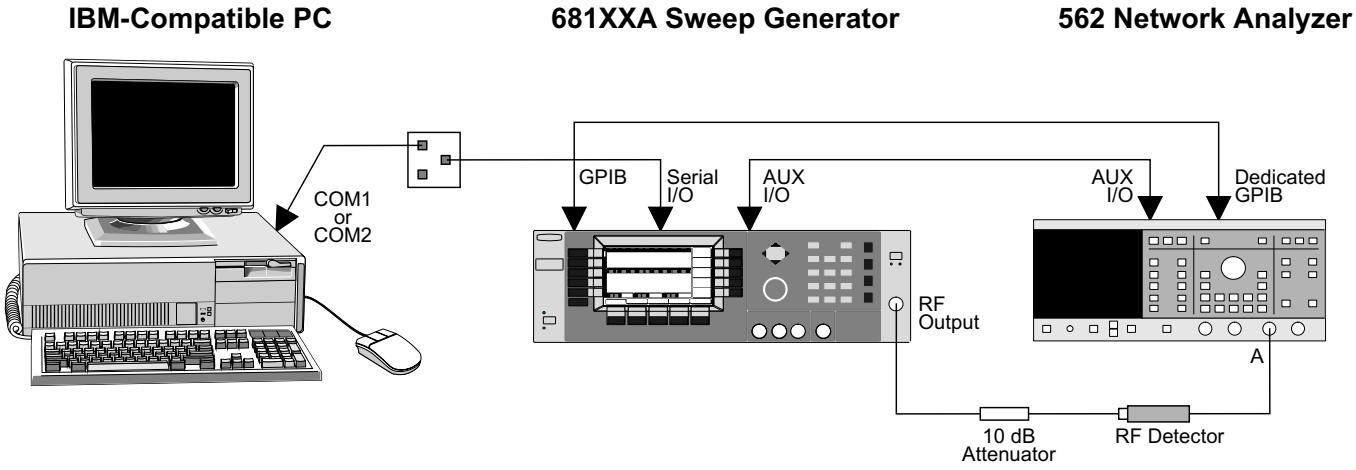


Figure 4-5. *Equipment Setup for ALC Slope Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-5, as follows:

1. Interface the PC to the 681XXA by performing the initial setup procedure, pages 4-7 to 4-10.
2. Using the Auxiliary I/O cable, connect the 681XXA rear panel AUX I/O connector to the 562 Network Analyzer AUX I/O connector.
3. Using the GPIB cable, connect the 562 Network Analyzer DEDICATED GPIB connector to the 681XXA IEEE-488 GPIB connector.
4. Connect the RF Detector to the 562 Network Analyzer Channel A Input connector.
5. Connect the 681XXA RF OUTPUT connector to the RF Detector via a 10 dB Attenuator.

NOTE

Before beginning this calibration procedure, *always* let the 681XXA warm up for a minimum of one hour.

ALC Slope DAC Adjustment

The following procedure lets you adjust the ALC Slope DAC to compensate for decreasing output power-vs-frequency for frequencies ≤2 GHz and for frequencies >2 GHz.

1. Set up the 562 Network Analyzer as follows:
   a. Press the System Menu key.
   b. From the System Menu display, select RESET.
   c. Press CHANNEL 2 DISPLAY: OFF
   d. Press CHANNEL 1 DISPLAY: ON
   e. Press CHANNEL 1 MENU key.
   f. From the Channel 1 Menu display, select TRANSMISSION and SELECT INPUT (NON-RATIO A).

Note

For instruments that do not contain a Down Converter (Models 68137A and 68163A), skip to step 6.

2. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit L1** and set L1 to 5 dB less than maximum leveled power for the instrument being calibrated (refer to Table 4-4).
   c. Press **Step** . The Step Sweep Menu is displayed.
   d. Press **Edit F1** and set the F1 start frequency to 0.01 GHz.
   e. Press **Edit F2** and set the F2 stop frequency to **2.1 GHz**.
   f. Press **Sweep Ramp** . At the resulting Step Sweep Ramp Menu, press **Num of Steps** and set the number of steps to 200.
   g. Press **Step** to return to the Step Sweep Menu display.

Table 4-4. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68137A	+13 dBm	+10 dBm
68147A	+13 dBm	+10 dBm
68163A	+6 dBm	+2 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68137A	+17 dBm	+14 dBm
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

3. Make the following selections on the 562 Network Analyzer to normalize the step sweep.
   a. Press CALIBRATION and follow the menu on the display.
   b. Press AUTOSCALE.
   c. Press OFFSET/RESOLUTION and set the Resolution to 0.2 dB.

4. On the 681XXA, press **Analog** to select the analog sweep mode.

5. Adjust the ALC Slope DAC for frequencies ≤2 GHz as follows:
   a. At the **$** prompt on the PC display, type: **drt_cal** and press <ENTER>. A menu is presented on the screen that lists all DACs and their current settings.
   b. Select item 19 (ALC Slope Het) from the menu. Follow the instructions presented at the bottom of the screen to enter a new DAC setting value.
   c. Enter different DAC setting values to find the setting that adjusts the slope so that the power at the start and stop frequencies match the normalized straight line in step sweep mode.
   d. When finished, exit the program.

6. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit L1** and set L1 to 5 dB less than maximum leveled power for the instrument being calibrated (refer to Table 4-4).
   c. Press **Step** . The Step Sweep Menu is displayed.
   d. Press **Edit F1** and set the F1 start frequency to 2.0 GHz.
   e. Press **Edit F2** and set the F2 stop frequency to 20.0 GHz for models 68137A and 68147A or 40 GHz for models 68163A and 68169A.
   f. Press **Sweep Ramp** . At the resulting Step Sweep Ramp Menu, press **Num of Steps** and set the number of steps to 200.
   g. Press **Step** to return to the Step Sweep Menu display.

7. Make the following selections on the 562 Network Analyzer to normalize the step sweep.
   a. Press CALIBRATION and follow the menu on the display.
   b. Press AUTOSCALE.
   c. Press OFFSET/RESOLUTION and set the Resolution to 0.2 dB.
8. On the 681XXA, press **Analog** to select the analog sweep mode.
9. Adjust the ALC Slope DAC for frequencies >2 GHz as follows:
   a. At the **$** prompt on the PC display, type: **drt_cal** and press <ENTER>. A menu is presented on the screen that lists all DACs and their current settings.
   b. Select item 20 (ALC Slope Main) from the menu. Follow the instructions presented at the bottom of the screen to enter a new DAC setting value.
   c. Enter different DAC setting values to find the setting that adjusts the slope so that the power at the start and stop frequencies match the normalized straight line in step sweep mode.
   d. When finished, exit the program.
10. Store the new DAC setting values as follows:
    a. At the **$** prompt, type the following:

       send 3 303 and press <ENTER>
       cal_code & and press <ENTER>
       calterm 787 and press <ENTER>

       The **$** prompt will appear on the screen when the data has been stored.
11. At the $ prompt, type: calterm 875 and press <ENTER> to exit the calibration program.
12. Turn the 681XXA off, then back on to return the instrument to normal operation.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-10 RF LEVEL CALIBRATION

RF level calibration requires the use of an automated test system. A computer-controlled power meter measures the 681XXA power output at many frequencies throughout the frequency range of the instrument. Correction factors are then calculated and stored in non-volatile memory (EEPROM) located on the A17 CPU PCB.

This calibration is required following replacement of either the A9 PIN Control PCB, the A9-1 PIN Control PCB, the A10 ALC PCB, the A14 Doubler Driver PCB, the Switched Filter Assembly, the Down Converter Assembly, the Frequency Extension Unit (FEU), the Switched Doubler Module (SDM), the Directional Coupler, or the Step Attenuator.

The RF level calibration software is available from WILTRON by ordering part number 2300-104. This calibration program warrants level accuracy specifications from maximum power to –70 dBm. For calibration below –70 dBm, the 681XXA must be returned to your WILTRON service center for calibration. The RF level calibration software comes on a 3.5-inch/ 1.44 Mbyte, MS-DOS formatted floppy disk.

For information concerning test equipment requirements and ordering the automated program, contact your WILTRON service center (refer to Table 1-5 on page 1-15).

4-11 AM BANDWIDTH CALIBRATION

This procedure provides the steps necessary to perform AM Bandwidth calibration. The AM Bandwidth is adjusted to compensate for gain variations of the modulator. The adjustment is performed for each frequency band. This provides a more consistent bandwith throughout the frequency range of the instrument.

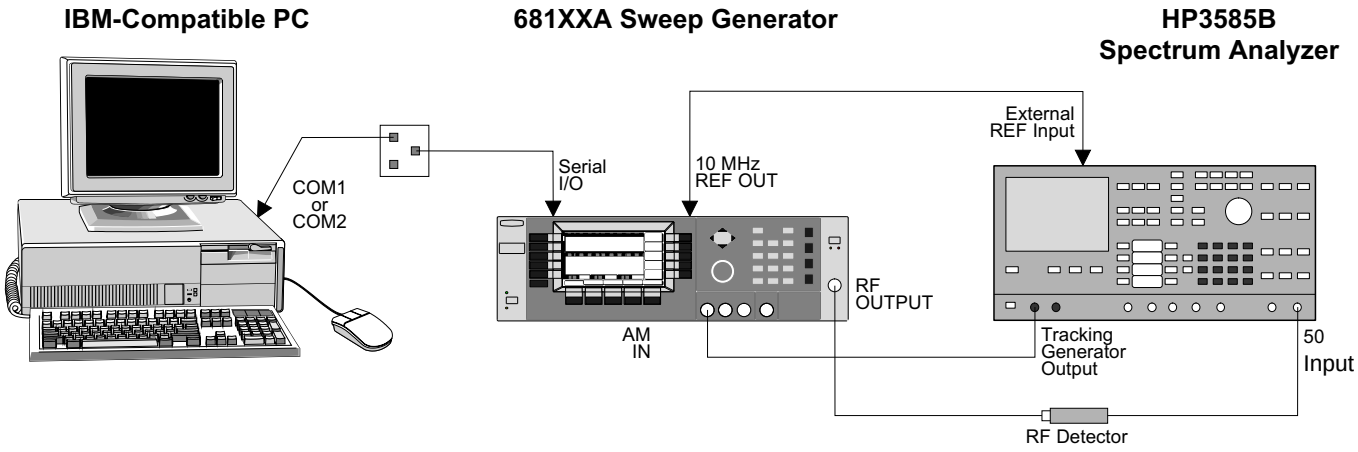


Figure 4-6. *Equipment Setup for AM Bandwidth Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-6, as follows:

1. Interface the PC to the 681XXA by performing the initial setup procedure, pages 4-7 to 4-10.
2. Connect the 681XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.
3. Connect the Spectrum Analyzer Tracking Generator Output to the 681XXA front panel AM IN.
4. Connect the RF Detector to the Spectrum Analyzer 50Ω input.
5. Connect the 681XXA RF OUTPUT to the RF Detector Input.

NOTE

Before beginning this calibration procedure, *always* let the 681XXA warm up for a minimum of one hour.

AM Bandwidth Adjustment

The following procedure lets you adjust the AM bandwidth to compensate for gain variations of the modulator throughout the instrument's frequency range .

1. Set up the Spectrum Analyzer as follows:
   a. Press the INSTR PRESET key.
   b. Press the START FREQ key and set the start frequency to 1 kHz.
   c. Press the STOP FREQ key and set the stop frequency to 200 kHz.
   d. Press the dB/div key and set for 1 dB.
   e. Press the REF LVL key to turn the reference level on.
   f. Press the AUTO RANGE key to turn auto range off.
   g. Press the REF LVL TRACKING key to turn referency level tracking off.

2. Set up the 681XXA as follows:
   a. Reset the instrument by pressing **SYSTEM** , then **Reset** . Upon reset the CW Menu is displayed.
   b. Press **Edit L1** and set L1 to 3 dB less than maximum leveled power for the instrument being calibrated (refer to Table 4-5).
   c. Press **MODULATION** , then **AM** . The External AM Status Menu is displayed.
   d. Press **On/Off** and select AM On.
   e. Press **Log/Linear** and select Linear mode (100%/V Sensitivity).
   f. Press **600Ω/50Ω** and select 50Ω impedance.
   g. Press **Front/Rear** and select Front Source.
   h. Press **CW/SWEEP SELECT** to return to the CW Menu display.

3. On the Spectrum Analyzer, adjust the control knob to display the waveform response.

Table 4-5. *Maximum Leveled Output Power*

Model Number	Output Power	Output Power with Option 2
68137A	+13 dBm	+10 dBm
68147A	+13 dBm	+10 dBm
68163A	+6 dBm	+2 dBm
68169A	+6 dBm	+2 dBm
With Option 15 (High Power) Installed		
68137A	+17 dBm	+14 dBm
68147A	+13 dBm, <2 GHz +17 dBm, ≥2 GHz	+10 dBm, <2 GHz +14 dBm, ≥2 GHz

4. On the 681XXA:
   a. Press **Edit F1** and set F1 to the start frequency of the first frequency band shown on the Test Record.
   b. Increment F1 in 100 MHz steps from the start frequency to locate the minimum bandwidth point. (The 3 dB points are 130 kHz for frequencies ≤20 GHz and 65 kHz for frequencies >20 GHz.)

5. Adjust the AM bandwidth as follows:
   a. At the **$** prompt on the PC display, type: **easy 42 128 8** and press <ENTER>.
   b. On the computer keyboard, use 1, 2, or 3 to increment and 8, 9, or 0 to decrement the value of the DAC's setting to achieve the desired bandwidth.
   c. Record the DAC's setting value on the Test Record.

6. Repeat steps 4 and 5 for each frequency band listed on the Test Record.

7. Exit the program by pressing **Q** on the keyboard.

Entering DAC Settings

The following procedure provides steps for entering the new DAC setting values into RAM located on the A17 CPU PCB.

1. Enter the new DAC setting values as follows:
   a. At the **$** prompt, type: **drct_cal** and press <ENTER>. A menu is presented on the screen that lists all DACs and their current settings.

   The following items from the menu pertain to the DAC settings for the frequency bands listed:

Item 21	Band 0 (0.01-2.0 GHz)
Item 22	Band 1 (2.0 -3.3 GHz)
Item 23	Band 2 (3.3-5.5 GHz)
Item 24	Band 3 (5.5-8.4 GHz)
Item 25	Band 4 (8.4-13.25 GHz)
Item 26	Band 5 (13.25-20.0 GHz)
Item 27	Band 6 (20-26.5 GHz w/FEU) (20-25 GHz w/SDM)
Item 28	Band 7 (26.5-33 GHz w/FEU) (25-32 GHz w/SDM)
Item 29	Band 8 (33-40 GHz w/FEU) (32-40 GHz w/SDM)

b. Select the item that pertains to the DAC setting to be updated. Following the instructions presented on the bottom of the screen, enter the new DAC setting value from the Test Record.

c. When you are finished entering all the new DAC setting values from the Test Record, exit the program.

Storing DAC Settings

The following procedure stores the new DAC setting values, entered above, in non-volatile memory (EEPROMs) located on the A17 CPU PCB.

1. Store the new DAC setting values as follows:
   a. At the **$** prompt, type the following:

      `send 3 303` and press <ENTER>
      `cal_code &` and press <ENTER>
      `calterm 787` and press <ENTER>

      The **$** prompt will appear on the screen when the data has been stored.

2. At the **$** prompt, type: **`calterm 875`** and press <ENTER> to exit the calibration program.

3. Turn the 681XXA off, then back on to return the instrument to normal operation.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-12 AM CALIBRATION

This procedure provides the steps necessary to perform AM calibration. The AM Calibration DAC is calibrated for input sensitivities of 100%/V (linear mode) and 10 dB/V (logarithmic mode) for frequencies ≤2 GHz and >2 GHz.

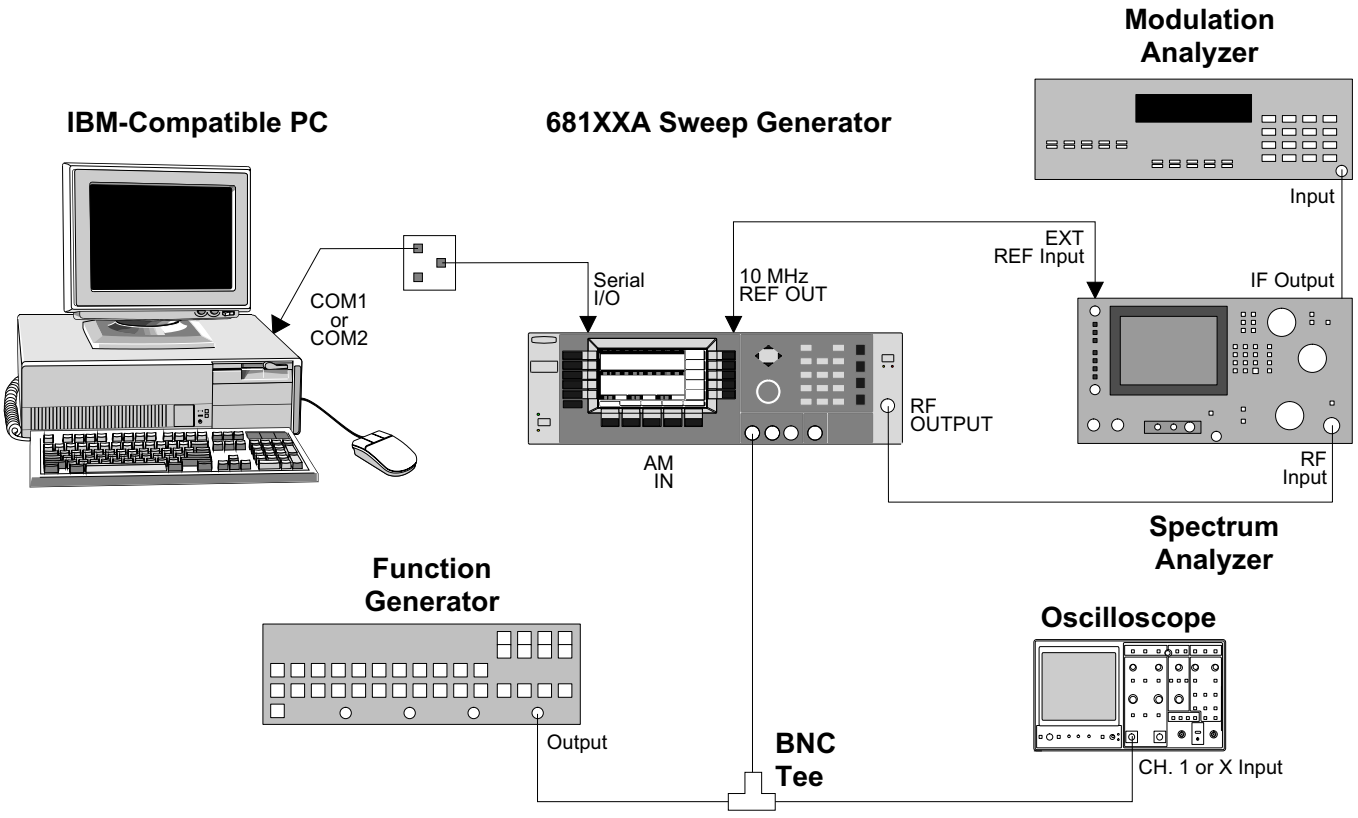


Figure 4-7. *Equipment Setup for AM Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-6, as follows:

1. Interface the PC to the 681XXA by performing the initial setup procedure, pages 4-7 to 4-10.

2. Connect the 681XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.

3. Connect the Function Generator Output to the BNC tee. Connect one leg of the tee to the 681XXA front panel AM IN. Connect the other leg of the tee to Oscilloscope CH.1 input (X input).

4. Connect the IF Output of the Spectrum Analyzer to the RF Input of the Modulation Analyzer.

5. Connect the 681XXA RF OUTPUT to the Spectrum Analyzer RF Input.

NOTE
Before beginning this calibration procedure, always let the 681XXA warm up for a minimum of one hour.

AM Calibration DAC Adjustment

The following procedure adjusts the AM Calibration DAC to provide the correct amount of AM in both linear (100%/V sensitivity) and log (10 dB/V) modes of operation for frequencies of ≤2 GHz and >2 GHz.

1. Set the Modulaton Analyzer as follows:
   a. MEASURE AM
   b. 300 Hz High-Pass Filter
   c. 3 kHz Low-Pass Filter

2. Perform Linear AM calibration as follows:
   a. At the **$** prompt on the PC screen, type the following:

      send 3 303 and press <ENTER>
      cal_code & and press <ENTER>
      calterm 112 and press <ENTER>

NOTE
For instruments that do not contain a Down Converter (Models 68137A and 68163A) skip to step 2. d.

   b. Set the Spectrum Analyzer Center Frequency to 1 GHz and follow the instructions on the screen. Use a 1 kHz sinewave with an amplitude of 1 volt peak-to-peak.
   c. When finished setting the DAC, press **Q** on the keyboard to go to the next screen display.
   d. Set the Spectrum Analyzer Center Frequency to 5 GHz and follow the instructions on the screen. Use a 1 kHz sinewave with an amplitude of 1 volt peak-to-peak.
   e. When finished setting the DAC, press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)

NOTE
To save the calibration data after completing any calibration step, type: **calterm 787** and press <ENTER>.

f. Record step completion on the Test Record.

3. Perform Log AM calibration as follows:
   a. At the **$** prompt, type: **calterm 113** and press <ENTER>.

NOTE
For instruments that do not contain a Down Converter (Models 68137A and 68163A) skip to step 2. d.

   b. Set the Spectrum Analyzer Center Frequency to 1 GHz and follow the instructions on the screen. Use a 1 kHz sinewave with an amplitude of 1 volt peak-to-peak.
   c. When finished setting the DAC, press **Q** on the keyboard to go to the next screen display.
   d. Set the Spectrum Analyzer Center Frequency to 5 GHz and follow the instructions on the screen. Use a 1 kHz sinewave with an amplitude of 1 volt peak-to-peak.
   e. When finished setting the DAC, press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)
   f. Record step completion on the Test Record.

4. Store the calibration data as follows:
   a. At the **$** prompt, type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)

5. At the **$** prompt, type: **calterm 875** and press <ENTER> to exit the calibration program.

6. Turn the 681XXA off, then back on to return the instrument to normal operation.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

4-13 FM CALIBRATION

This procedure provides the steps necessary to perform FM calibration. FM calibration consists of calibrating the FM Meter circuit and adjusting the FM Calibration DAC for input sensitivities of 20 MHz/V, 10 MHz/V, and –6 MHz/V in both narrow and wide FM modes.

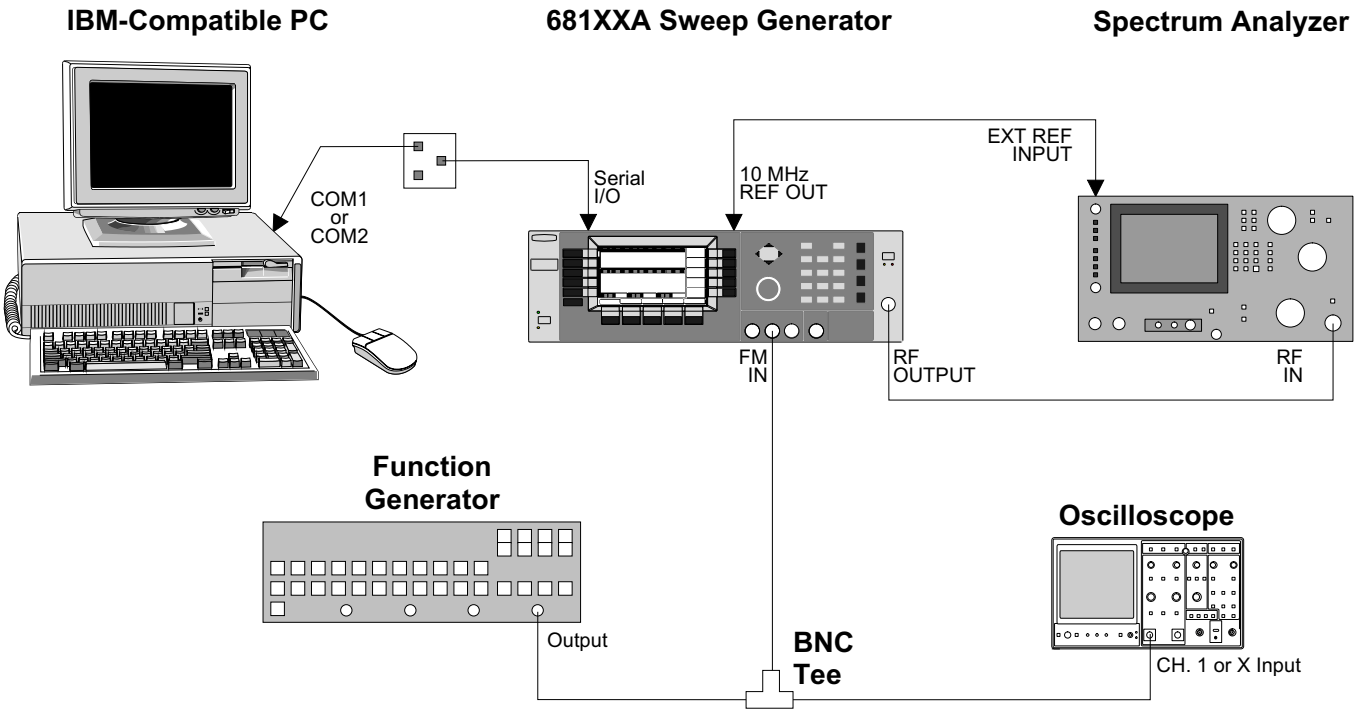


Figure 4-8. *Equipment Setup for FM Calibration*

Equipment Setup

Connect the equipment, shown in Figure 4-8, as follows:

1. Interface the PC to the 681XXA by performing the intial setup procedure, pages 4-7 to 4-10.

2. Connect the 681XXA rear panel 10 MHz REF OUT to the Spectrum Analyzer External Reference Input.

3. Connect the Function Generator Output to the BNC tee. Connect one leg of the tee to the 681XXA front panel FM IN. Connect the other leg of the tee to Oscilloscope CH.1 input (X input).

4. Connect the 681XXA RF OUTPUT to the Spectrum Analyzer RF Input.

NOTE

Before beginning this calibration procedure, always let the 681XXA warm up for a minimum of one hour.

FM Calibration Procedure

The following procedure lets you calibrate the FM Meter circuit, adjust the FM Calibration DAC in both narrow and wide modes, and store the results in non-volatile memory (EEPROMs) on the A17 CPU PCB.

1. Set up the Spectrum Analyzer as follows:
   a. Center Frequency: 5 GHz
   b. Span/Div: 10 MHz/Div

NOTE

To ensure accurate calibration, each step of this procedure must be performed in sequence.

2. Perform FM Meter calibration as follows:
   a. At the **$** prompt on the PC screen, type the following:

      send 3 303 and press <ENTER>
      cal_code & and press <ENTER>
      calterm 123 and press <ENTER>

   b. Follow the instructions on the screen. Use a 100 kHz sinewave with an amplitude of 1 volt peak-to-peak.

      The **$** prompt will appear on the screen when the calibration is complete.

   c. Record step completion on the Test Record.

NOTE

To save the calibration data after completing any calibration step, type: **calterm 787** and press <ENTER>.

3. Perform FM Wide Sensitivity calibration as follows:
   a. At the **$** prompt, type: **calterm 124** and press <ENTER>.
   b. Follow the instructions on the screen. Use a 0.5 Hz square wave with an amplitude of 1 volt peak.
   c. When finished setting the DAC, press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)
   d. Record step completion on the Test Record.

4. Perform FM Narrow Sensitivity calibration as follows:
   a. At the **$** prompt, type: **calterm 125** and press <ENTER>.
   b. Follow the instructions on the screen. Use a 0.5 Hz square wave with an amplitude of 1 volt peak.
   c. When finished setting the DAC, press **Q** on the keyboard to exit the program. (The **$** prompt will appear on the screen.)
   d. Record step completion on the Test Record.
5. Store the calibration data as follows:
   a. At the **$** prompt, type: **calterm 787** and press <ENTER>. (The **$** prompt will appear on the screen when the calibration data has been stored.)
6. At the **$** prompt, type: **calterm 875** and press <ENTER> to exit the calibration program.
7. Turn the 681XXA off, then back on to return the instrument to normal operation.

CAUTION

When saving calibration data, turning off the instrument before the **$** prompt returns to the screen can cause all stored data to be lost.

Chapter 5
Troubleshooting

Table of Contents

The majority of the troubleshooting procedures presented in this chapter require the removal of the instrument covers to gain access to test points on printed circuit boards and other subassemblies.

WARNING

Hazardous voltages are present inside the 681XXA whenever ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Troubleshooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many subassemblies in the 681XXA contain static-sensitive components. Improper handling of these subassemblies may result in damage to the components. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-4.

Chapter 5
Troubleshooting

5-1 INTRODUCTION

This chapter provides information for troubleshooting sweep generator malfunctions. The troubleshooting procedures presented in this chapter support fault isolation to a replaceable subassembly or RF component. (Remove and replace procedures for the subassemblies and RF components are found in Chapter 6.)

5-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for the troubleshooting procedures presented in this chapter is listed in Chapter 1, Table 1-2 (page 1-10).

5-3 ERROR AND WARNING/STATUS MESSAGES

During normal operation, the 681XXA generates error messages to indicate internal malfunctions, abnormal signal generator operations, or invalid signal inputs or data entries. It also displays warning messages to alert the operator to conditions that could result in inaccurate sweep generator output. In addition, status messages are displayed to remind the operator of current menu selections or settings.

Self-Test Error Messages

The 681XXA firmware includes internal diagnostics that self-test the instrument. These self-test diagnostics perform a brief go/no-go test of most of the instrument PCBs and other internal assemblies.

You can perform a sweep generator self-test at any time during normal operation by pressing **SYSTEM** and then the System Menu soft-key **Selftest** .

If the sweep generator fails self-test, an error message(s) is displayed on the front panel data display. These error messages describe the malfunction and, in most cases, provide an indication of what has failed. Table 5-1 is a summary listing of the self-test error messages. Included for each is a reference to the troubleshooting table that provides a description of the probable cause(s) and a procedure for identifying the failed component or assembly.

Table 5-1. *Self-Test Error Messages (1 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 100 DVM Ground Offset Failed	5-5	5-13
Error 101 DVM Positive 10V Reference	5-5	5-13
Error 102 DVM Negative 10V Reference	5-5	5-13
Error 105 Power Supply Voltage(s) out of Regulation	5-6	5-14
Error 106 Power Supply not Locked	5-6	5-23
Error 107 Sweep Time Check Failed	5-16	5-31
Error 108 Crystal Oven Cold	5-8	5-24
Error 109 The 100MHz Reference is not Locked to the External Reference	5-8	5-24
Error 110 The 100MHz Reference is not Locked to the High Stability 10MHz Crystal Oscillator	5-8	5-25
Error 111 Fine Loop Osc Failed	5-9	5-25
Error 112 Coarse Loop Osc Failed	5-11	5-27
Error 113 Yig Loop Osc Failed	5-13	5-28
Error 114 Down Converter LO not Locked	5-14	5-29
Error 115 Not Locked Indicator Failed	5-13	5-28
Error 116 FM Loop Gain Check Failed	5-15	5-30
Error 117 Linearizer Check Failed	5-16	5-31
Error 118 Switchpoint DAC Failed	5-16	5-31
Error 119 Center Frequency Circuits Failed	5-16	5-31

Table 5-1. *Self-Test Error Messages (2 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 120 Delta-F Circuits Failed	5-16	5-31
Error 121 Unleveled Indicator Failed	5-17	5-32
Error 122 Level Reference Failed	5-17	5-32
Error 123 Detector Log Amp Failed	5-17	5-32
Error 124 Full Band Unlocked and Unleveled	5-18	5-34
Error 125 8.4 – 20 GHz Unlocked and Unleveled	5-18	5-34
Error 126 2 – 8.4 GHz Unlocked and Unleveled	5-18	5-34
Error 127 Detector Input Circuit Failed	5-17	5-32
Error 128 .01 – 2 GHz Unleveled	5-20	5-36
Error 129 Switched Filter or Level Detector Failed	5-20	5-38
Error 130 2 – 3.3 GH Switched Filter	5-20	5-40
Error 131 3.3 – 5.5 GH Switched Filter	5-20	5-40
Error 132 5.5 – 8.4 GH Switched Filter	5-20	5-40
Error 133 8.4 – 13.25 GH Switched Filter	5-20	5-40
Error 134 13.25 – 20 GH Switched Filter	5-20	5-40
Error 135 Modulator or Driver Failed	5-20	5-41
Error 142 Sample and Hold Circuit Failed	5-17	5-32
Error 143 Slope DAC Failed	5-17	5-33

Table 5-1. *Self-Test Error Messages (3 of 3)*

Error Message	Troubleshooting Table	Page Number
Error 144 RF was Off when Selftest started. Some tests were not performed.	5-26	5-48
681XXA Models with FEU		
Error 136 26.5 – 40 GHz Modulator or Driver Failed	5-22	5-42
Error 137 20 – 26.5 GHz Modulator or Driver Failed	5-22	5-42
Error 138 FEU Unit or Driver Failed	5-22	5-43
Error 139 33 – 40 GHz FEU Section Failed	5-22	5-45
Error 140 26 – 33 GHz FEU Section Failed	5-22	5-45
Error 141 20 – 26 GHz FEU Section Failed	5-22	5-45
681XXA Models with SDM		
Error 138 SDM Unit or Driver Failed	5-24	5-46
Error 139 32 – 40 GHz SDM Section Failed	5-24	5-46
Error 140 25 – 32 GHz SDM Section Failed	5-24	5-46
Error 141 20 – 25 GHz SDM Section Failed	5-24	5-46

Normal Operation Error and Warning/ Status Messages

When an abnormal condition is detected during operation, the 681XXA displays an error message to indicate that the output is abnormal or that a signal input or data entry is invalid. It also displays warning messages to alert the operator to conditions that could cause an inaccurate signal generator output. Status messages to remind the operator of current menu selections or settings are also generated.

Table 5-2 is a summary list of possible error messages that can be displayed during normal operations. Table 5-3 is a summary list of possible warning/status messages.

Table 5-2. *Possible Error Messages during Normal Operations*

Error Message	Description
ERROR	Displayed (on the frequency mode title bar) when (1) the output frequency is not phase-locked or (2) an invalid entry causes a frequency range error.
LOCK ERROR	Displayed (in the frequency parameters area) when the output frequency is not phase-locked. The frequency accuracy and stability of the RF output is greatly reduced. Normally caused by an internal component failure. Run self-test to verify malfunction.
RANGE ERR	Displayed (in the frequency parameters area) when (1) the sweep start frequency entered is greater than the stop frequency, (2) the ΔF value entered results in a sweep outside the range of the instrument, (3) the step size value entered is greater than the sweep range, or (4) the number of steps entered results in a step size of less than 1 kHz (0.1 Hz with Option 11). Entering valid values usually clears the error.
ERR	Displayed (in the modulation status area) when either the external AM modulating signal or the external FM modulating signal exceeds the input voltage range. In addition, the message "**Reduce AM (FM) Input Level**" appears at the bottom of the AM (FM) status display. AM (FM) will be turned off until the modulating signal is in the input voltage range.

Table 5-3. *Possible Warning/Status Messages during Normal Operation*

Warning/Status Message	Description
OVN COLD	This warning message indicates that the 100 MHz Crystal oven (or the 10 MHz Crystal oven if Option 16 is installed) has not reached operating temperature. Normally displayed during a cold start of the sweep generator. If the message is displayed during normal operation, it could indicate a malfunction. Run self-test to verify.
UNLEVELED	Displayed when the RF output goes unleveled. Normally caused by exceeding the specified leveled-power rating. Reducing the power level usually clears the warning message. If the warning message is displayed only when AM is selected ON, the modulating signal may be driving the RF output unleveled. Reducing the modulating signal or adjusting the power level usually clears the warning.
UNLOCKED	When FM is selected ON, this warning message appears indicating that the instrument is not phase-locked during the FM mode of operation.
EXT REF	This status message indicates that an external 10 MHz signal is being used as the reference signal for the 681XXA.
OFFSET	This status message indicates that a constant (offset) has been applied to the displayed power level.
SLOPE	This status message indicates that a power slope correction has been applied to the ALC.

5-4 MALFUNCTIONS NOT DISPLAYING AN ERROR MESSAGE

The 681XXA must be operating to run self-test. Therefore, malfunctions that cause the instrument to be non-operational do not produce error messages. These problems generally are a failure of the 681XXA to power up properly. Table 5-4, beginning on page 5-11, provides troubleshooting procedures for these malfunctions.

5-5 TROUBLESHOOTING TABLES

Tables 5-4 through 5-23, beginning on page 5-11, provide procedures for isolating malfunctions to a replaceable subassembly or RF component. In those cases where any of several subassemblies or RF components could have caused the problem, subassembly/RF component replacement is indicated. The recommended replacement order is to replace first the subassemblies/RF components that are most likely to have failed.

Figure 5-1, on the following page, shows the location of the 681XXA connectors and test points that are called out in the troubleshooting procedures of Tables 5-4 through 5-23.

CAUTION

Never remove or replace a subassembly or RF component with power applied. Serious damage to the instrument may occur.

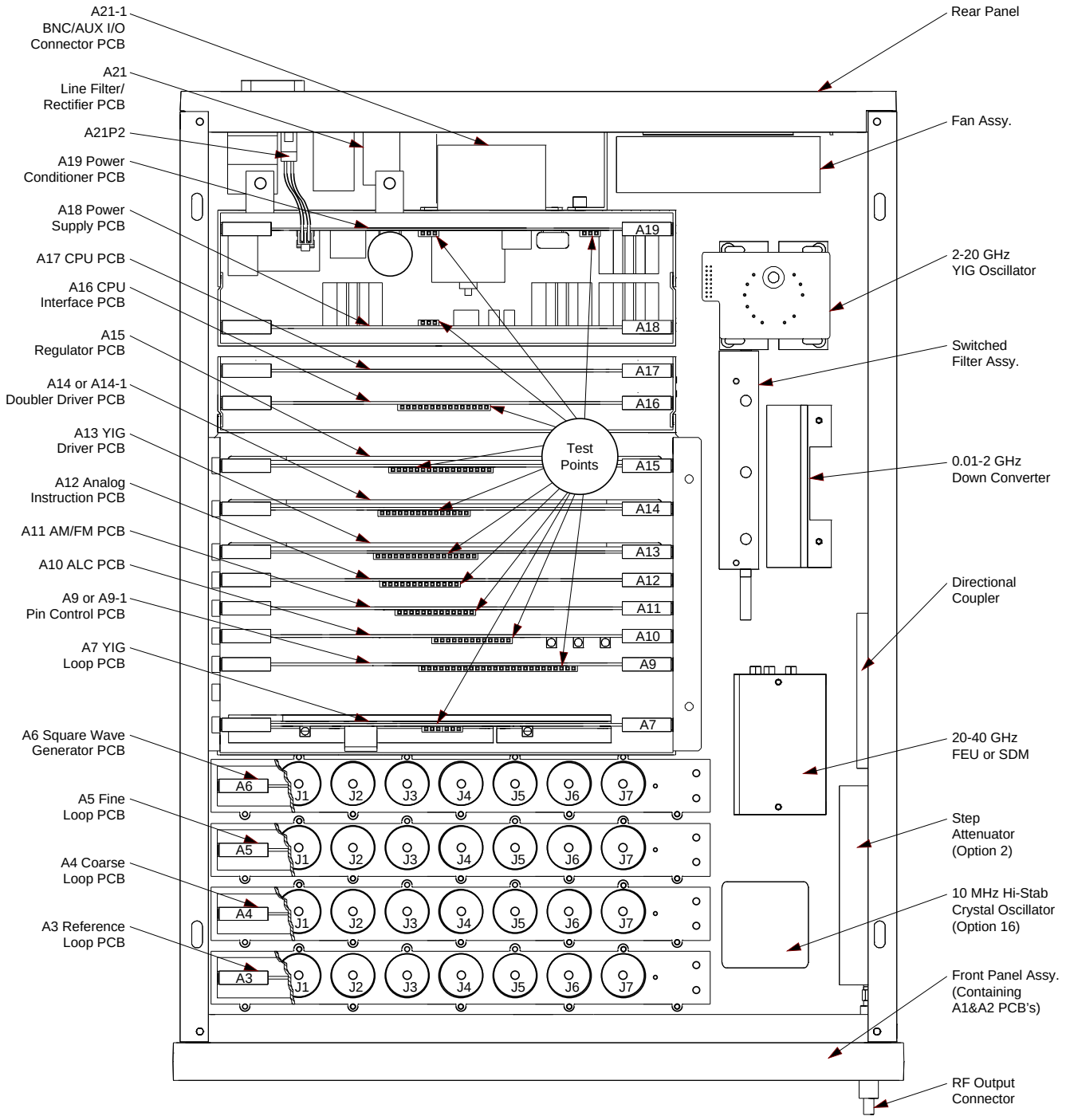


Figure 5-1. *Top View of the 681XXA Showing Connector and Test Point Locations*

Table 5-4. *Malfunctions Not Displaying an Error Message (1 of 2)*

Sweep Generator Will Not Turn On (OPERATE light is OFF)

Normal Operation: When the 681XXA is connected to the power source, the OPERATE light should illuminate and the instrument should power up.

Step 1. Disconnect the 681XXA from the power source, then check the fuses and fuse holders in the rear panel line voltage module.

- ☐ If they are good, go to step 2.
- ☐ If a fuse(s) or fuse holder(s) is defective, replace but do **not** apply power. Go to step 2.

Step 2. Remove the 681XXA top cover and the safety cover located over the Line Filter assembly and A21 Line Rectifier PCB that are located on the rear panel.

Step 3. Disconnect the cable at connector A21P2.

Step 4. Connect a DVM across the pins 1 and 2 of A21P2, then connect the 681XXA to the power source. Check for a 330 volt reading on the DVM.

- ☐ If the voltage is correct, go to step 5.
- ☐ If the voltage is incorrect or the fuses blow, replace the A21 PCB.

Step 5. Disconnect the 681XXA from the power source and allow time for the capacitors on the A21 PCB to discharge.

Step 6. Reconnect the cable at A21 P2, then remove the cover over the A18 and A19 PCBs.

Step 7. After connecting the negative lead of the DMM to A19TP3 and the positive lead to A19TP2, connect the 681XXA to the power source and check for a +28 ±2 volt reading on the DMM.

- ☐ If the voltage is correct, go to step 8.
- ☐ If the voltage is incorrect or the fuses blow, replace the A19 PCB.

Step 8. Connect the negative lead of the DMM to A15TP1 and the positive lead to A15TP14, check for a +23.33 ±0.5 volts reading on the DMM.

Table 5-4. *Malfunctions Not Displaying an Error Message (2 of 2)*

- ☐ If the voltage is correct, the Front Panel assembly or the cable between Motherboard connector A20J2 and the Front Panel assembly may be defective.
- ☐ If the voltage is incorrect, the +24V standby power supply may be loaded down by (1) a shorted oven heater for the 100 MHz reference oscillator located on the A3 PCB, (2) a shorted heater for the optional 10 MHz high stability time base (if installed), or (3) a defective Front Panel assembly.

Sweep Generator Will Not Turn On (OPERATE light is ON)

Normal Operation: When the 681XXA is connected to the power source, the OPERATE light should illuminate and the instrument should power up.

Step 1. Remove the 681XXA top cover and the cover over the A18 and A19 PCBs.

Step 2. Connect the negative lead of the DMM to A18TP1 and the positive lead to A18TP3.

Step 3. Check for a +23.3 ±0.5 volt reading on the DMM.

- ☐ If the voltage is correct, go to step 4.
- ☐ If the voltage is incorrect or missing, the Front Panel assembly or the cable between Motherboard connector A20J2 and the Front Panel assembly may be defective.

Step 4. Press the front panel RF OUTPUT ON/OFF button. Do the yellow and red LEDs toggle?

- ☐ If yes, the malfunction may be caused by a failed front panel circuit. Replace the Front Panel assembly.
- ☐ If the LEDs do not toggle or if both LEDs are lit, the problem may be caused by a malfunction on the A16 CPU Interface PCB or the A17 CPU PCB.

Table 5-5. *Error Messages 100, 101, and 102*

Internal DVM Tests

Error 100 DVM Ground Offset Failed, *or*
Error 101 DVM Positive 10V Reference, *or*
Error 102 DVM Negative 10V Reference

Description: The DVM circuitry, located on the A16 CPU Interface PCB, is calibrated using the ±10 volts from the reference supplies on the A12 Analog Instruction PCB. The error messages indicate a calibration-related problem or a defective ±10 volt reference.

Step 1. Perform a manual pre-calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, 100, 101, and 102, are displayed, go to step 3.

Step 3. Connect the negative lead of the digital multimeter to A12TP1.

Step 4. Measure the ±10V reference voltages at A12TP4 and A12TP8. A12TP4 should be –10V ±0.036V; A12TP8 should be +10V ±0.036V.

- ☐ If the ±10V reference voltages are correct, go to step 5.
- ☐ If incorrect, replace the A12 PCB.

NOTE

Even if the ±10V reference voltages are correct, there could still be a malfunction of the DVM multiplexer on the A12 PCB or the DVM circuitry on the A16 CPU Interface PCB.

Step 5. Replace the A12 PCB and run self-test again.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, 100, 101, and 102, are displayed, go to step 6.

Step 6. Replace the A16 PCB, then run self-test.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, 100, 101, and 102, are displayed, contact your local WILTRON service center for assistance.

Table 5-6. *Error Messages 105 and 106 (1 of 10)*

Power Supply Tests

WARNING

Voltages hazardous to life are present throughout the power supply circuits, *even when the front panel* LINE *switch is in the* STANDBY *postion*. When performing maintenance, use utmost care to avoid electrical shock.

Error 105 Power Supply Voltage(s) out of Regulation.

Description: The out of regulation circuit, located on the A15 Regulator PCB, monitors all of the regulated power supply outputs. This error message indicates that one of more of the voltages from the power supply, with the exception of the 5 volt supply, is out of regulation. If the 5 volt supply is faulty, the 681XXA will not operate.

Step 1. Measure the regulated voltages at the test points shown in Table 5-7.

- ☐ If incorrect for a supply, go to the referenced step.
- ☐ If incorrect for several supplies, go to step 2.
- ☐ If all voltages are correct, go to step 3.

Table 5-7. *Regulated Power Supply Voltages*

Regulated Voltage	Measurement Point	Reference Point	Value	Refer to Step
+15VG	A15 TP3	A15 TP1	+15V ±0.75V	4
–15VG	A15 TP9	A15 TP1	–15V ±0.75V	4
+15VA	A15 TP2	A15 TP1	+15 ±0.75V	5
–15VA	A15 TP7	A15 TP1	–15V ±0.75V	5
+15VLP	A15 TP12	A15 TP1	+15V ±0.75V	6
–15VLP	A15 TP13	A15 TP1	–15V ±0.75V	6
+15VFM	A15 TP8	A15 TP1	+15V ±0.75V	7
–15VFM	A15 TP11	A15 TP1	–15V ±0.75V	7
–18VT	A15 TP10	A15 TP1	–18V ±0.36V	8
–43VT	A15 TP15	A15 TP1	–43V ±0.9V	9
+24VH	A15 TP6	A15 TP1	+24.32V ±0.5V	10

Table 5-6. *Error Messages 105 and 106 (2 of 10)*

Step 2. Perform the following procedure to isolate malfunctions when the voltages from several regulated supplies are incorrect.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the regulated voltages per Table 5-7.

- ☐ If the voltages are correct, the problem is cleared.
- ☐ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Replace the A18 PCB.

f. Place the LINE switch to OPERATE and measure the regulated voltages per Table 5-7.

- ☐ If the voltages are correct, the problem is cleared.
- ☐ If the voltages are still incorrect, contact your local WILTRON service center for assistance.

Step 3. Run self-test again.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If error 105 displays again, contact your local WILTRON service center for assistance.

Table 5-6. *Error Messages 105 and 106 (3 of 10)*

±15VG Supply Problems

This supply provides ±15 volts to the YIG Driver, Doubler Driver, SDM Driver, CPU, and CPU I/O circuits and the Switched Filter and Down Converter assemblies.

Step 4. Perform the following procedure to isolate malfunctions to the ±15VG supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VG voltages per Table 5-7.

☐ If the voltages are correct, the problem is cleared.

☐ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13, A14, A16, and A17 PCBs as applicable for your model.

f. Place the LINE switch to OPERATE and measure the ±15VG voltages.

☐ If the voltages are correct, go to step j.

☐ If the voltages are still incorrect, go to step g.

g. Place the LINE switch to STANDBY.

h. Remove the switched filter and down converter assemblies.

i. Place the LINE switch to OPERATE and measure the ±15VG voltages.

☐ If the voltages are correct, go to step j.

☐ If the voltages are still incorrect, contact your local WILTRON service center for assistance.

j. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

k. Place the LINE switch to OPERATE and measure the ±15VG voltages.

l. Continue steps j and k until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (4 of 10)*

±15VA Supply Problems

This supply provides ±15 volts to the PIN Control, ALC, AM/FM Driver, and Analog Instruction circuits.

Step 5. Perform the following procedure to isolate malfunctions to the ±15VA supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VA voltages per Table 5-7.

- ☐ If the voltages are correct, the problem is cleared.
- ☐ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A9, A10, A11, and A12 PCBs.

f. Place the LINE switch to OPERATE and measure the ±15VA voltages.

- ☐ If the voltages are correct, go to step g.
- ☐ If the voltages are still incorrect, contact your local WILTRON service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

h. Place the LINE switch to OPERATE and measure the ±15VA voltages.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (5 of 10)*

±15VLP Supply Problems

This supply provides ±15 volts to the Reference, Coarse, Fine, and YIG Phase-Lock Loop circuits.

Step 6. Perform the following procedure to isolate malfunctions to the ±15VLP supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VLP voltages per Table 5-7.

- ☐ If the voltages are correct, the problem is cleared.
- ☐ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A3, A4, A5, and A7 PCBs.

f. Place the LINE switch to OPERATE and measure the ±15VLP voltages.

- ☐ If the voltages are correct, go to step g.
- ☐ If the voltages are still incorrect, contact your local WILTRON service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs/assemblies.

h. Place the LINE switch to OPERATE and measure the ±15VLP voltages.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (6 of 10)*

±15VFM Supply Problems

This supply provides ±15 volts to the FM portion of the YIG Driver circuits.

Step 7. Perform the following procedure to isolate malfunctions to the ±15VFM supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the ±15VLP voltages per Table 5-7.

- ☐ If the voltages are correct, the problem is cleared.
- ☐ If the voltages are incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13 PCB.

f. Place the LINE switch to OPERATE and measure the ±15VLP voltages.

- ☐ If the voltages are correct, replace the A13 PCB.
- ☐ If the voltages are still incorrect, contact your local WILTRON service center for assistance.

Table 5-6. *Error Messages 105 and 106 (7 of 10)*

–18VT Supply Problems

This supply provides –18 volts to drive the YIG-tuned oscillator main tuning coil during CW and slow analog sweeps.

Step 8. Perform the following procedure to isolate malfunctions to the –18VT supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the –18VT voltage per Table 5-7.

- ☐ If the voltage is correct, the problem is cleared.
- ☐ If the voltage is incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A13 PCB and the YIG-tuned oscillator assembly.

f. Place the LINE switch to OPERATE and measure the –18VT voltage.

- ☐ If the voltage is correct, go to step g.
- ☐ If the voltage is still incorrect, contact your local WILTRON service center for assistance.

g. Place the LINE switch to STANDBY.

h. Install the A13 PCB.

i. Place the LINE switch to OPERATE and measure the –18VT voltage.

- ☐ If the voltage is correct, replace the YIG-tuned oscillator assembly.
- ☐ If the voltage is incorrect, replace the A13 PCB.

Table 5-6. *Error Messages 105 and 106 (8 of 10)*

–43VT Supply Problems

This supply provides –43 volts to drive the YIG-tuned oscillator main tuning coil during bandswitching, fast analog sweeps, and digital sweeps.

Step 9. Perform the following procedure to isolate malfunctions to the –43VT supply and its outlying load circuit.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE.

d. Set up the 681XXA to perform a 2 to 20 GHz step sweep.

e. Measure the –43VT voltage per Table 5-7.

- ☐ If the voltage is correct, the problem is cleared.
- ☐ If the voltage is incorrect, go to step f.

f. Place the LINE switch to STANDBY.

g. Remove the A13 PCB and the YIG-tuned oscillator assembly.

h. Place the LINE switch to OPERATE and measure the –43VT voltage.

- ☐ If the voltage is correct, go to step i.
- ☐ If the voltage is still incorrect, contact your local WILTRON service center for assistance.

i. Place the LINE switch to STANDBY.

j. Install the A13 PCB.

k. Place the LINE switch to OPERATE and measure the –43VT voltage.

- ☐ If the voltage is correct, replace the YIG-tuned oscillator assembly.
- ☐ If the voltage is incorrect, replace the A13 PCB.

Table 5-6. *Error Messages 105 and 106 (9 of 10)*

+24VH Supply Problems

This supply provides +24 volts for the YIG-tuned oscillator heater, the V/GHz circuit on the A12 PCB, and coarse and fine loop circuits. When the 681XXA is switched to OPERATE, it also takes over the function of the 24VS supply and supplies +24 volts to the 100 MHz reference oscillator oven heater, the front panel LINE switch circuitry, and the optional 10 MHz high stability time base oven heater.

Step 10. Perform the following procedure to isolate malfunctions to the +24VH supply and outlying load circuits.

a. Place the LINE switch to STANDBY.

b. Replace the A15 PCB assembly.

c. Place the LINE switch to OPERATE and measure the +24VH voltage per Table 5-7.

- ☐ If the voltage is correct, the problem is cleared.
- ☐ If the voltage is incorrect, go to step d.

d. Place the LINE switch to STANDBY.

e. Remove the A4, A5, and A12 PCBs and the YIG-tuned oscillator assembly.

f. Place the LINE switch to OPERATE and measure the +24VH voltage.

- ☐ If the voltage is correct, go to step g.
- ☐ If the voltage is still incorrect, contact your local WILTRON service center for assistance.

g. Place the LINE switch to STANDBY, then install one of the removed PCBs or the YIG-tuned oscillator assembly.

h. Place the LINE switch to OPERATE and measure the +24VH voltage.

i. Continue steps g and h until the faulty PCB/assembly is located.

Table 5-6. *Error Messages 105 and 106 (10 of 10)*

Power Supply Not Phase-Locked

Error 106 Power Supply not Locked

Description: The switching power supply is not phase locked to the 400 kHz reference signal from the A6 Square Wave Generator PCB.

Step 1. Using an oscilloscope, verify the presence of a 400 kHz TTL square wave at TP4 on the A6 PCB.

- ☐ If present, replace the A18 Power Supply PCB.
- ☐ If not present, go to step 2.

Step 2. Set up the 681XXA for internal square wave modulation.

Step 3. Using an oscilloscope, verify the presence of a TTL square wave at the TP3 on the A6 PCB.

- ☐ If present, replace the A6 PCB.
- ☐ If not present, go to step 4.

Step 4. Using an oscilloscope, verify the presence of a 10 MHz TTL signal at J4 of the A5 Fine Loop PCB.

- ☐ If present, go to step 5.
- ☐ If not present, go to step 6.

Step 5. Check the cable, W108, that goes between A5J4 and A6J1.

- ☐ If the cable is good, replace the A6 PCB.
- ☐ If the cable has failed, replace it.

Step 6. Using a spectrum analyzer, verify the presence of a +3 dBm ±5 dB, 10 MHz signal at J3 of the A3 Reference Loop PCB.

- ☐ If present, go to step 7.
- ☐ If not present, replace the A3 PCB.

Step 7. Check the cable, W104, that goes between A3J3 and A5J5.

- ☐ If the cable is good, replace the A5 PCB.
- ☐ If the cable has failed, replace it.

Table 5-8. *Error Messages 108, 109 and 110 (1 of 2)*

A3 Reference Loop

Error 108 Crystal Oven Cold

Description: The oven of the 100 MHz crystal oscillator or the Option 16 high-stability 10 MHz crystal oscillator has not reached operating temperature.

Step 1. Allow a 30 minute warm up, then run self-test again.

- ☐ If error 108 is not displayed, the problem is cleared.
- ☐ If error 108 displays and Option 16 is not installed, replace the A3 PCB.
- ☐ If error 108 displays and Option 16 is installed, go to step 2.

Step 2. Disconnect the cable A20P4 that goes to the Option 16 crystal oscillator assembly.

Step 3. Run self-test again.

- ☐ If error 108 is not displayed, replace the Option 16 crystal oscillator assembly.
- ☐ If error 108 is still displayed, replace the A3 PCB.

Error 109 The 100MHz Reference is not phase-locked to the External Reference

Description: The reference loop is not phase-locked to the external 10 MHz reference.

Step 1. Using a coaxial cable with BNC connectors, connect the rear panel 10 MHz REF IN connector to the rear panel 10 MHz REF OUT connector.

Step 2. Disconnect the cable, W110, from A3J7.

Step 3. Using an oscilloscope, verify the presence of a 10 MHz signal at the end of the cable. The signal amplitude should be >0.5 volts peak-to-peak (into 50Ω).

- ☐ If present, replace the A3 PCB.
- ☐ If not present, replace the cable W110.

Table 5-8. *Error Messages 108, 109 and 110 (2 of 2)*

Error 110 The 100MHz Reference is not Locked to the High Stability 10MHz Crystal Oscillator

Description: The reference loop is not phase-locked to the Option 16 high stability 10 MHz crystal oscillator.

Step 1. Disconnect the cable from A3J6.

Step 2. Using an oscilloscope, verify the presence of a 10 MHz signal at the end of the cable. The signal amplitude should be ≥1 volt (into 50Ω).

- ☐ If present, replace the A3 PCB.
- ☐ If not present, replace the Option 16 crystal oscillator.

Table 5-9. *Error Message 111*

A5 Fine Loop

Error 111 Fine Loop Osc Failed

Description: One or more of the oscillators within the fine loop is not phase-locked.

Step 1. Disconnect cable W104 at A5J5.

Step 2. Using a spectrum analyzer, verify the presence of a +3 dBm ±5 dB, 10 MHz signal at the end of the cable.

- ☐ If present, go to step 3.
- ☐ If not present, replace the A3 PCB.

Step 3. Reconnect cable W104 to A5J5 and disconnect cable W107 at A5J1.

Step 4. Set up the 681XXA to generate the CW frequencies listed in Table 5-10.

Step 5. Using a spectrum analyzer, measure the frequency and amplitude of the signal at A5J1 for each of the CW frequencies generated. In each case, the signal amplitude should be +3 dBm ±3 dB with sidebands at <–65 dBc.

- ☐ If the signals are correct in both frequency and amplitude, go to step 6.
- ☐ If the signals are incorrect, replace the A5 PCB.

Step 6. Reconnect cable W107 to A5J1 and run self-test again.

- ☐ If error 111 is not displayed, the problem is cleared.
- ☐ If error 111 is still displayed, contact your local WILTRON service center for assistance.

Table 5-10. *Fine Loop Frequencies*

681XXA CW Frequency	Measured Frequency at A5J1
10.102 GHz	22 MHz
10.110 GHz	30 MHz
10.120 GHz	40 MHz

Table 5-11. *Error Message 112*

A4 Coarse Loop

Error 112 Coarse Loop Osc Failed

Description: The coarse loop oscillator is not phase-locked.

Step 1. Disconnect cable W103 at A4J1 and cable W105 at A4J6.

Step 2. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 500 MHz signal at the end of cable W103 and a +3 dBm ±5 dB, 10 MHz signal at the end of cable W105.

- ☐ If present, go to step 3.
- ☐ If not present, replace the A3 PCB.

Step 3. Reconnect cable W103 to A4J1 and cable W105 to A4J6, then disconnect cable W106 at A4J3.

Step 4. Set up the 681XXA to generate the CW frequencies listed in Table 5-12.

Step 5. Using a spectrum analyzer, measure the frequency and amplitude of the signal at A4J3 for each of the CW frequencies generated. In each case, the signal amplitude should be +4 dBm ±6 dB with sidebands at <–50 dBc.

- ☐ If the signals are correct in both frequency and amplitude, go to step 6.
- ☐ If the signals are incorrect, replace the A4 PCB.

Step 6. Reconnect cable W106 to A4J3 and run self-test again.

- ☐ If error 112 is not displayed, the problem is cleared.
- ☐ If error 112 is still displayed, contact your local WILTRON service center for assistance.

Table 5-12. *Coarse Loop Frequencies*

681XXA CW Frequency	Measured Frequency at A4J3
2.000 GHz	439 MHz ±10 kHz
2.050 GHz	450 MHz ±10 kHz
2.225 GHz	489 MHz ±10 kHz

Table 5-13. *Error Messages 113 and 115 (1 of 2)*

A7 YIG Loop

Error 113 YIG Loop Osc Failed
Error 115 Not Locked Indicator Failed

Description: Error 113 indicates that the YIG loop is not phase-locked. Error 115 indicates a failure of the not phased-lock indicator circuit.

Step 1. Verify the signal output from the A4 Coarse Loop PCB by performing steps 3 thru 5 in Table 5-11.

- ☐ If the coarse loop signals are correct in both frequency and amplitude, go to step 2.
- ☐ If the coarse loop signals are incorrect, replace the A4 PCB.

Step 2. Verify the signal output from the A5 Fine Loop PCB by performing steps 3 thru 5 in Table 5-9.

- ☐ If the fine loop signals are correct in both frequency and amplitude, go to step 3.
- ☐ If the fine loop signals are incorrect, replace the A5 PCB.

Step 3. Disconnect the semi-rigid cable at output port J5 of the switched filter assembly.

Step 4. Set up the 681XXA to generate a CW frequency of 2.000 GHz.

Step 5. Using a spectrum analyzer, measure the frequency and amplitude of the signal at J5 of the switched filter assembly. The frequency should be 2.000 GHz ±25 MHz and the amplitude should be from –20 to –27 dBm.

- ☐ If the signal is correct in both frequency and amplitude, go to step 6.
- ☐ If the signals are incorrect, replace the switched filter assembly.

Step 6. Repeat steps 4 and 5, incrementing the CW frequency in 1 GHz steps up to 20.000 GHz.

Step 7. If the signals from the coarse loop, fine loop, and switched filter assembly are all correct, replace the A7 YIG Loop PCB.

Table 5-13. *Error Messages 113 and 115 (2 of 2)*

Step 8. Run self-test.

- ☐ If error 113 or 115 are not displayed, the problem is cleared.
- ☐ If either error 113 or 115 are displayed, contact your local WILTRON service center for assistance.

Table 5-14. *Error Message 114*

Down Converter

Error 114 Down Converter LO not Locked

Description: The local oscillator in the down converter assembly is not phase-locked.

Step 1. Disconnect cable W112 at A3J2.

Step 2. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 500 MHz signal at A3J2.

- ☐ If present, go to step 3.
- ☐ If not present, replace the A3 PCB.

Step 3. Reconnect cable W112 to A3J1, then disconnect cable W112 at J2 of the down converter assembly.

Step 4. Using a spectrum analyzer, verify the presence of a +5 dBm ±6 dB, 500 MHz signal at the end of cable W112.

- ☐ If present, replace the down converter assembly.
- ☐ If not present, replace cable W112.

Table 5-15. *Error Message 116 (1 of 2)*

A11 AM/FM PCB

Error 116 FM Loop Gain Check Failed

Description: The FM loop has failed or the loop gain is out of tolerance. During self-test, the fine loop is offset 10 MHz and the internal DVM checks for a 1 volt offset at the output of A11 AM/FM PCB.

Step 1. Perform a manual pre-calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ☐ If error 116 is not displayed, the problem is cleared.
- ☐ If error 116 is still displayed, go to step 3.

Step 3. Set up the 681XXA as follows:

a. CW frequency: 5 GHz

b. Modulation: External FM On [Unlocked]
Mode: Narrow
Sensitivity: 10 MHz/V

Step 4. Apply a 1 volt peak-to-peak sine wave to the FM IN BNC connector.

Step 5. Using an oscilloscope, check for a 1 volt peak-to-peak signal at A11TP10.

- ☐ If the test signal is present, go to step 6.
- ☐ If the test signal is not present or is incorrect, replace the A11 PCB.

Step 6. Using an oscilloscope, check for a 1 volt peak-to-peak signal at A13TP11.

- ☐ If the test signal is present, go to step 7.
- ☐ If the test signal is not present or is incorrect, replace the A13 PCB.

NOTE

Even if the test signals in steps 5 and 6 are both correct, the problem could still be caused by a malfunction on the A5 or A11 PCB.

Table 5-15. *Error Message 116 (2 of 2)*

Step 7. Replace the A11 PCB and run self-test again.

- ☐ If error 116 is not displayed, the problem is cleared.
- ☐ If error 116 is still displayed, go to step 8.

Step 8. Replace the A5 PCB and run self-test again.

- ☐ If error 116 is not displayed, the problem is cleared.
- ☐ If error 116 is displayed, contact your local WILTRON service center for assistance.

Table 5-16. *Error Messages 107, 117, 118, 119, and 120*

A12 Analog Instruction

Error 107 Sweep Time Check Failed
Error 117 Linearizer Check Failed
Error 118 Switchpoint DAC Failed
Error 119 Center Frequency Circuits Failed
Error 120 Delta-F Circuits Failed

Description: Each of these error messages indicates a problem in the circuitry on the A12 Analog Instruction PCB that provides frequency tuning voltages for the YIG-tuned oscillator.

Step 1. Perform a manual pre-calibration. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, listed above, is displayed, go to step 3.

Step 3. Replace the A12 PCB and run self-test again.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, listed above, is displayed, contact your local WILTRON service center for assistance.

Table 5-17. *Error Messages 121, 122, 123, 127, 142, and 143 (1 of 2)*

A10 ALC

Error 121 Unleveled Indicator Failed
Error 122 Level Reference Failed
Error 123 Detector Log Amp Failed
Error 127 Detector Input Circuit Failed

Description: Error 121 indicates a failure of the circuit that alerts the CPU whenever the RF output power becomes unleveled. Each of the other error messages indicates a problem in the circuitry on the A10 ALC PCB that provides control of the RF output power level.

Step 1. Replace the A10 PCB, and run self-test.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, listed above, is displayed, contact your local WILTRON service center for assistance.

Error 142 Sample and Hold Circuit Failed

Description: Error 142 indicates a failure of the sample and hold circuitry on the A10 PCB.

Step 1. Set up the 681XXA as follows:

a. Modulation: Square Wave On
Source: Internal
Frequency: 400 Hz
Polarity: High RF On

Step 2. Using an oscilloscope, check for a 400 Hz square wave signal at A9TP13.

- ☐ If the signal is present, replace the A10 PCB.
- ☐ If the signal is not present, go to step 3.

Step 3. Using the oscilloscope, check for a 400 Hz square wave signal at A6TP3.

- ☐ If the signal is present, replace the A9 PCB.
- ☐ If the signal is not present, replace the A6 PCB.

Table 5-17. Error Messages 121, 122, 123, 127, 142, and 143 (2 of 2)

Error 143 Slope DAC Failed

Description: Error 143 indicates a problem with the level slope DAC circuitry on the A10 PCB.

Step 1. Recalibrate the ALC slope. (Refer to chapter 4 for the calibration procedure.)

Step 2. Run self-test.

- ☐ If error 143 is not displayed, the problem is cleared.
- ☐ If error 143 is still displayed, go to step 3.

Step 3. Replace the A10 PCB and run self-test again.

- ☐ If error 143 is not displayed, the problem is cleared.
- ☐ If error 143 is still displayed, go to step 4.

Step 4. Replace the A12 PCB and run self-test again.

- ☐ If error 143 is not displayed, the problem is cleared.
- ☐ If error 143 is still displayed, contact your local WILTRON service center for assistance.

Table 5-18. *Error Messages 124, 125, and 126 (1 of 2)*

YIG-tuned Oscillator

Error 124 Full Band Unlocked and Unleveled
Error 125 8.4-20 GHz Unlocked and Unleveled
Error 126 2-8.4 GHz Unlocked and Unleveled

Description: These error messages indicate either a failure of one or both of the oscillators in the 2-20 GHz YIG-tuned oscillator assembly.

Step 1. Connect a 562 Scalar Network Analyzer to the 681XXA as follows:

a. Connect the 681XXA AUX I/O to the 562 AUX I/O.

b. Connect the 562 DEDICATED GPIB to the 681XXA IEEE-488 GPIB.

c. Connect the RF Detector to the 562 Channel A Input.

Step 2. Set up the 681XXA as follows:

a. Sweep Select: Analog
F1: 2.000 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec

Step 3. Set up the 562 Scalar Network Analyzer as follows:

a. Press SYSTEM MENU key.

b. From System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF

d. Press CHANNEL 1 DISPLAY: ON

e. Press CHANNEL 1 MENU key.

f. From the Channel 1 Menu display, select POWER.

Step 4. Using the scalar network analyzer, measure the RF output directly at the YIG-tuned oscillator's output connector. The amplitude of the RF signal should be >4 dBm throughout the full sweep.

☐ If the RF signal is correct in both frequency and amplitude throughout the full analog sweep, go to step 8.

☐ If there is no RF signal for all or part of the analog sweep or if the amplitude of the RF signal is low, go to step 5.

Step 5. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Table 5-18. *Error Messages 124, 125, and 126 (2 of 2)*

Step 6. Using the oscilloscope, check for a –0.2 to –3.5 volt YIG tuning ramp at A13TP10.

- ☐ If the ramp signal is correct, go to step 7.
- ☐ If the ramp signal is incorrect or not present, replace the A13 PCB.

Step 7. Using the oscilloscope, check for the YIG bias voltages at the test points shown in Table 5-19.

- ☐ If the YIG bias voltages are correct, replace the YIG-tuned oscillator assembly.
- ☐ If the YIG bias voltages are incorrect, replace the A13 PCB.

Step 8. Run self-test again.

- ☐ If no error message is displayed, the problem is cleared.
- ☐ If any of the error messages, listed above, is displayed, contact your local WILTRON service center for assistance.

Table 5-19. *YIG-tuned Oscillator Bias Voltages*

Test Point	YIG-tuned Oscillator Bias Voltages	
	2 to 8.4 GHz	8.4 to 20 GHz
A13TP3	+6V	+6V
A13TP5	0V	+8V
A13TP6	–5V	–5V
A13TP7	+8V	0V

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (1 of 6)*

Output Power Level Related Problems (0.01 to 20 GHz)

Error 128 .01-2 GHz Unleveled

Description: Error 128 indicates a failure of of the down converter leveling circuitry. The 681XXA may or may not produce an RF output in the 0.01 to 2 GHz frequency range. Thus, there are two troubleshooting paths for this problem—unleveled with output power and unleveled with no/low output power.

Unleveled with output power (The warning message **UNLEVELED** appears on the front panel display):

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 2.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: External Detector

Step 2. Connect a detector to the 681XXA RF OUTPUT connector and connect the detected DC output of the detector to the front panel EXTERNAL ALC IN connector.

- ☐ If the warning message **UNLEVELED** no longer appears on the front panel display, replace the down converter.
- ☐ If the warning message **UNLEVELED** is still displayed, replace the A10 PCB.

Unleveled with no/low output power:

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 0.010 GHz
F2: 2.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: Internal

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (2 of 6)*

Step 3. Using the oscilloscope, check at the end of the cable that is connected to A10J3 for a >0.7 volt down converter detector output throughout the full sweep.

If the detector voltage is correct, replace the A10 PCB.

If the detector voltage is incorrect, go to step 4.

Step 4. Using the oscilloscope, check for a +15 volt down converter bias voltage at A13TP14.

- ☐ If the bias voltage is correct, go to step 5.
- ☐ If the bias voltage is not correct, replace the A13 PCB.

Step 5. Using the oscilloscope, check for a –2 volt PIN switch drive voltage at A9TP19. If the 681XXA has a FEU installed, also check for a –4 volt PIN switch drive voltage at A9TP9.

- ☐ If the PIN switch drive voltage(s) is correct, go to step 6.
- ☐ If the PIN switch drive voltage(s) is not correct, replace the A9 PCB.

Step 6. Connect a 562 Scalar Network Analyzer to the 681XXA as follows:

- **a.** Connect the 681XXA AUX I/O to the 562 AUX I/O.
- **b.** Connect the 562 DEDICATED GPIB to the 681XXA IEEE-488 GPIB.
- **c.** Connect the RF Detector to the 562 Channel A Input.

Step 7. Set up the 562 Scalar Network Analyzer as follows:

- **a.** Press SYSTEM MENU key.
- **b.** From System Menu display, select RESET.
- **c.** Press CHANNEL 2 DISPLAY: OFF
- **d.** Press CHANNEL 1 DISPLAY: ON
- **e.** Press CHANNEL 1 MENU key.
- **f.** From the Channel 1 Menu display, select POWER.

Step 7. Using the scalar network analyzer, measure the RF output at J3 of the switched filter assembly. The amplitude of the RF signal should be >0 dBm throughout the full sweep.

- ☐ If the amplitude of the RF signal is correct, replace the down converter assembly.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (3 of 6)*

- ☐ If there is no RF signal or if the amplitude of the RF signal is low, replace the switched filter assembly.

Error 129 Switched Filter or Level Detector Failed

Description: Error 129 indicates a failure of either the switched filter or level detector circuitry. The 681XXA may or may not produce an RF output in the 2 to 20 GHz frequency range. Thus, there are two troubleshooting paths for this problem—unleveled with output power and unleveled with no/low output power.

Unleveled with output power (The warning message **UNLEVELED** appears on the front panel display):

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 2.000 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: External Detector

Step 2. Connect a detector to the 681XXA RF OUTPUT connector and connect the detected DC output of the detector to the front panel EXTERNAL ALC IN connector.

- ☐ If the warning message **UNLEVELED** no longer appears on the front panel display, replace the directional coupler.
- ☐ If the warning message **UNLEVELED** is still displayed, replace the A10 PCB.

Unleveled with no/low output power:

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 2.000 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: Internal

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (4 of 6)*

Step 3. Using the oscilloscope, check the switched filter bias voltages at A13TP4 and A13TP9. The bias voltage at A13TP4 should be +6 volts; the bias voltage at A13TP9 should be +8 volts.

- ☐ If the bias voltages are correct, go to step 4.
- ☐ If the bias voltages are not correct, replace the A13 PCB.

Step 4. Connect a 562 Scalar Network Analyzer to the 681XXA as follows:

- **a.** Connect the 681XXA AUX I/O to the 562 AUX I/O.
- **b.** Connect the 562 DEDICATED GPIB to the 681XXA IEEE-488 GPIB.
- **c.** Connect the RF Detector to the 562 Channel A Input.

Step 5. Set up the 562 Scalar Network Analyzer as follows:

- **a.** Press SYSTEM MENU key.
- **b.** From System Menu display, select RESET.
- **c.** Press CHANNEL 2 DISPLAY: OFF
- **d.** Press CHANNEL 1 DISPLAY: ON
- **e.** Press CHANNEL 1 MENU key.
- **f.** From the Channel 1 Menu display, select POWER.

Step 6. Using the scalar network analyzer, measure the RF output at J2 of the switched filter assembly. The amplitude of the RF signal should be >+15 dbm (>+20 dBm with Option 15) throughout the full sweep.

- ☐ If the amplitude of the RF signal is correct, check for bad cables.
- ☐ If there is no RF signal or if the amplitude of the RF signal is low, replace the switched filter assembly.

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (5 of 6)*

Error 130 2-3.3 GH Switched Filter
Error 131 3.3-5.5 GH Switched Filter
Error 132 5.5-8.4 GH Switched Filter
Error 133 8.4-13.25 GH Switched Filter
Error 134 13.25-20 GH Switched Filter

Description: Each of these error messages indicates a failure in a switched filter path within the switched filter assembly. The 681XXA may or may not produce an RF output in the frequency range of the failed switched filter path.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 2.000 GHz
F2: 20.000 GHz
Sweep Time: 0.100 Sec

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check for the switched filter PIN switch drive voltages at the test points shown in Table 5-21.

- ☐ If the PIN switch drive voltages are correct, replace the switched filter assembly.
- ☐ If the PIN switch drive voltages are incorrect, replace the A9 PCB.

Table 5-21. *Switched Filter PIN Switch Drive Voltages*

Test Point	Active Frequency Range	Active Voltage	Inactive Voltage
A9TP18	2 to 3.3 GHz	–2V	+1V
A9TP10	3.3 to 5.5 GHz	–2V	+1V
A9TP12	5.5 to 8.4 GHz	–2V	+1V
A9TP16	8.4 to 13.25 GHz	–2V	+1V
A9TP21	13.25 to 20 GHz	–2V	+1V
A9TP17	2 to 8.4 GHz	–2V	+1V

Table 5-20. *Error Messages 128, 129, 130, 131, 132, 133, 134, and 135 (6 of 6)*

Error 135 Modulator or Driver Failed

Description: Error 135 indicates a failure of the modulator in the switched filter assembly or the modulator driver circuitry on the A9 PIN Control PCB.

Step 1. Replace the A9 PCB and run self-test.

- ☐ If error 135 is not displayed, the problem is cleared.
- ☐ If error 135 is still displayed, go to step 2.

Step 2. Replace the switched filter assembly and run self-test again.

- ☐ If error 135 is not displayed, the problem is cleared.
- ☐ If error 135 is still displayed, contact your local WILTRON service center for assistance.

Table 5-22. *Error Messages 136, 137, 138, 139, 140, and 141 (1 of 4)*

Output Power Level Related Problems (20 to 40 GHz) 681XXA Models with FEU

Error 136 26.5 to 40 GHz Modulator or Driver Failed
Error 137 20 to 26.5 GHz Modulator or Driver Failed

Description: Each of these error messages indicates a failure of a modulator in the FEU or a failure of the modulator driver circuitry on the A14 Doubler Driver PCB. The 681XXA may or may not produce an RF output in the frequency range of the failed modulator.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

b. LEVEL/ALC SELECT: ALC Mode
Leveling Menu: External Detector

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the modulator driver voltages at A14TP10 and A14TP11.
A14TP10: When unleveled, approximately 9 volts when sweeping from 20 to 26.5 GHz.
A14TP11: When unleveled, approximately 9 volts when sweeping from 26.5 to 40 GHz.

☐ If the modulator driver voltages are correct, go to step 4.

☐ If the modulator driver voltages are not correct, replace the A14 PCB.

Step 4. Connect a detector to the 681XXA RF OUTPUT connector and connect the detected DC output of the detector to the front panel EXTERNAL ALC IN connector.

Step 5. Using the oscilloscope, check the modulator driver voltages at A14TP10 and A14 TP11 again.
A14TP10: Approximately 5 volts when sweeping from 20 to 26.5 GHz.
A14TP11: Approximately 5 volts when sweeping from 26.5 to 40 GHz.

Table 5-22. *Error Messages 136, 137, 138, 139, 140, and 141 (2 of 4)*

- ☐ If the modulator driver voltages do not change, replace the FEU.
- ☐ If the modulator driver voltages change as described, contact your local WILTRON service center for assistance.

Error 138 FEU Unit or Driver Failed

Description: Error 138 indicates a failure of the FEU, a failure of the FEU bias regulator circuitry on the A14 Doubler Driver PCB, or an incorrect RF signal level from the switched filter assembly. The 681XXA will not produce an RF output in the 20 to 40 GHz frequency range.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the FEU bias voltages at A14TP5, A14TP3, and A14TP6.
A14TP5: +12 volts when sweeping from 20 to 26.5 GHz.
A14TP3: +12 volts when sweeping from 26.5 to 33 GHz.
A14TP6: +12 volts when sweeping from 33 to 40 GHz.

- ☐ If the FEU bias voltages are correct, go to step 4.
- ☐ If the FEU bias voltages are not correct, replace the A14 PCB.

Step 4. Connect a 562 Scalar Network Analyzer to the 681XXA as follows:

a. Connect the 681XXA AUX I/O to the 562 AUX I/O.

b. Connect the 562 DEDICATED GPIB to the 681XXA IEEE-488 GPIB.

c. Connect the RF Detector to the 562 Channel A Input.

Step 5. Set up the 562 Scalar Network Analyzer as follows:

a. Press SYSTEM MENU key.

b. From System Menu display, select RESET.

c. Press CHANNEL 2 DISPLAY: OFF

Table 5-22. *Error Messages 136, 137, 138, 139, 140, and 141 (3 of 4)*

d. Press CHANNEL 1 DISPLAY: ON

e. Press CHANNEL 1 MENU key.

f. From the Channel 1 Menu display, select POWER.

Step 6. Using the scalar network analyzer, measure the RF output at J4 of the switched filter assembly.
When sweeping from 10 to 13.25 GHz, the amplitude of the RF signal should be >+18 dbm.
When sweeping from 13.25 to 20 GHz, the amplitude of the RF signal should be >16 dBm.

- ☐ If the amplitude of the RF signal is low, replace the switched filter assembly.
- ☐ If there is no RF signal output from J4, go to step 7.
- ☐ If the amplitude of the RF signal is correct, go to step 8.

Step 7. Using the oscilloscope, check for a –2 volts PIN switch drive voltage at A9TP19 throughout the full sweep.

- ☐ If the PIN switch drive voltage is correct, replace the switched filter assembly.
- ☐ If the PIN switch drive voltage is not correct, go to step 8.

Step 8. Replace the A9 PCB and run self-test again.

- ☐ If error 138 is not displayed, the problem is cleared.
- ☐ If error 138 is still displayed, go to step 9.

Step 9. Replace the FEU and run self-test again.

- ☐ If error 138 is not displayed, the problem is cleared.
- ☐ If error 138 is still displayed, contact your local WILTRON service center for assistance.

Table 5-22. *Error Messages 136, 137, 138, 139, 140, and 141 (4 of 4)*

Error 139 33-40 GHz FEU Section Failed
Error 140 26-33 GHz FEU Section Failed
Error 141 20-26 GHz FEU Section Failed

Description: Each of these error messages indicates a failure in a doubler/amplifier path within the FEU. The 681XXA will not produce an RF output in the frequency range of the failed doubler/amplifier.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the FEU bias voltages at A14TP5, A14TP3, and A14TP6.
A14TP5: +12 volts when sweeping from 20 to 26.5 GHz.
A14TP3: +12 volts when sweeping from 26.5 to 33 GHz.
A14TP6: +12 volts when sweeping from 33 to 40 GHz.

☐ If the FEU bias voltages are correct, go to step 4.

☐ If the FEU bias voltages are not correct, replace the A14 PCB.

Step 4. Using the oscilloscope, check the PIN switch drive voltages at A9TP26, A9TP25, and A9TP24 (shown in Table 5-23).

☐ If the PIN switch drive voltages are correct, replace the FEU.

☐ If the PIN switch drive voltages are incorrect, replace the A9 PCB.

Table 5-23. *FEU PIN Switch Drive Voltages*

Test Point	Active Frequency Range	Active Voltage	Inactive Voltage
A9TP9	0.01 to 2 GHz	–4V	+2V
A9TP11	2 to 33 GHz	–3V	+2V
A9TP15	2 to 20 GHz	–3V	+2V
A9TP24	33 to 40 GHz	–2V	+2V
A9TP26	20 to 26.5 GHz	–3V	+2V
A9TP25	26.5 to 33 GHz	–2V	+2V

Table 5-24. *Error Messages 138, 139, 140, and 141 (1 of 2)*

Output Power Level Related Problems (20 to 40 GHz) 681XXA Models with SDM

Error 138 SDM Unit or Driver Failed

Description: Error 138 indicates a failure of the SDM, a failure of the SDM bias regulator circuitry on the A14-1 SDM Driver PCB, or a failure of the frequency band selection circuitry on the A12 Analog Instruction PCB. The 681XXA will not produce an RF output in the 20 to 40 GHz frequency range.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check for a +8 volts SDM bias voltage at A14-1TP2 throughout the full sweep.

☐ If the SDM bias voltage is correct, replace the SDM.

☐ If the SDM bias voltage is not correct, go to step 4.

Step 4. Replace the A14-1 PCB and run self-test again.

☐ If error 138 is not displayed, the problem is cleared.

☐ If error 138 is still displayed, go to step 5.

Step 5. Replace the A12 PCB and run self-test again.

☐ If error 138 is not displayed, the problem is cleared.

☐ If error 138 is still displayed, contact your local WILTRON service center for assistance.

Table 5-24. Error Messages 138, 139, 140, and 141 (2 of 2)

Error 139 32-40 GHz SDM Section Failed
Error 140 25-32 GHz SDM Section Failed
Error 141 20-25 GHz SDM Section Failed

Description: Each of these error messages indicates a failure in a switched doubler filter path within the SDM. The 681XXA will not produce an RF output in the frequency range of the failed switched doubler filter path.

Step 1. Set up the 681XXA as follows:

a. CW/SWEEP SELECT: Analog
F1: 20.000 GHz
F2: 40.000 GHz
Sweep Time: 0.100 Sec
L1: +1.00 dBm

Step 2. Connect the X input of an oscilloscope to the 681XXA rear panel HORIZ OUT connector.

Step 3. Using the oscilloscope, check the PIN switch drive voltages at A9-1TP11, A9-1TP15, and A9-1TP24 (shown in Table 5-25).

- ☐ If the PIN switch drive voltages are correct, replace the SDM.
- ☐ If the PIN switch drive voltages are not correct, replace the A9-1 PCB.

Table 5-25. SDM PIN Switch Drive Voltages

Test Point	Active Frequency Range	Active Voltage	Inactive Voltage
A9-1TP9	0.01 to 2 GHz	+20V	–15V
A9-1TP11	20 to 25 GHz	+20V	–15V
A9-1TP15	25 to 32 GHz	+20V	–15V
A9-1TP24	32 to 40 GHz	+20V	–15V

Table 5-26. *Error Message 144*

Error 144 RF was Off when Selftest started. Some tests where not performed

Description: Indicates that some self-test where not performed because the RF Output was selected OFF on the front panel.

Step 1. Press the OUTPUT key on the front panel to turn the RF Output ON.

Step 2. Run self-test again.

Chapter 6
Removal and Replacement Procedures

Table of Contents

Chapter 6
Removal and Replacement Procedures

6-1 INTRODUCTION

This chapter provides procedures for gaining access to the major 681XXA assemblies, subassemblies, and components for calibration, troubleshooting, or replacement.

WARNING

Hazardous voltages are present inside the 681XXA whenever ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Troubleshooting and repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many subassemblies in the 681XXA contain static-sensitive components. Improper handling of these subassemblies may result in damage to the components. ***Always*** observe the static-sensitive component handling procedures described in Chapter 1, Figure 1-4.

6-2 REMOVING AND REPLACING THE CHASSIS COVERS

Calibration and troubleshooting procedures require removal of the top cover. Replacement of some 681XXA assemblies and parts require removal of all covers. The following procedure describes this process.

Preliminary Disconnect the power cord from the unit.

Procedure Remove and replace the chassis covers as follows:

Step 1 Loosen the screws and remove the two feet from the top corners at the rear of the instrument (Figure 6-1).

Step 2 Carefully slide the top cover out along the grooves in the chassis.

Step 3 Lift the top cover off and set it aside.

Step 4 Turn the instrument over so that the bottom cover is on top.

Step 5 Loosen the screws and remove the two feet from the bottom corners at the rear of the instrument.

Step 6 Carefully slide the bottom cover out along the grooves in the chassis.

Step 7 Lift the bottom cover off and set it aside.

Step 8 Turn the instrument over to return it to the upright position.

Step 9 To replace the covers, reverse the procedure used to remove them.

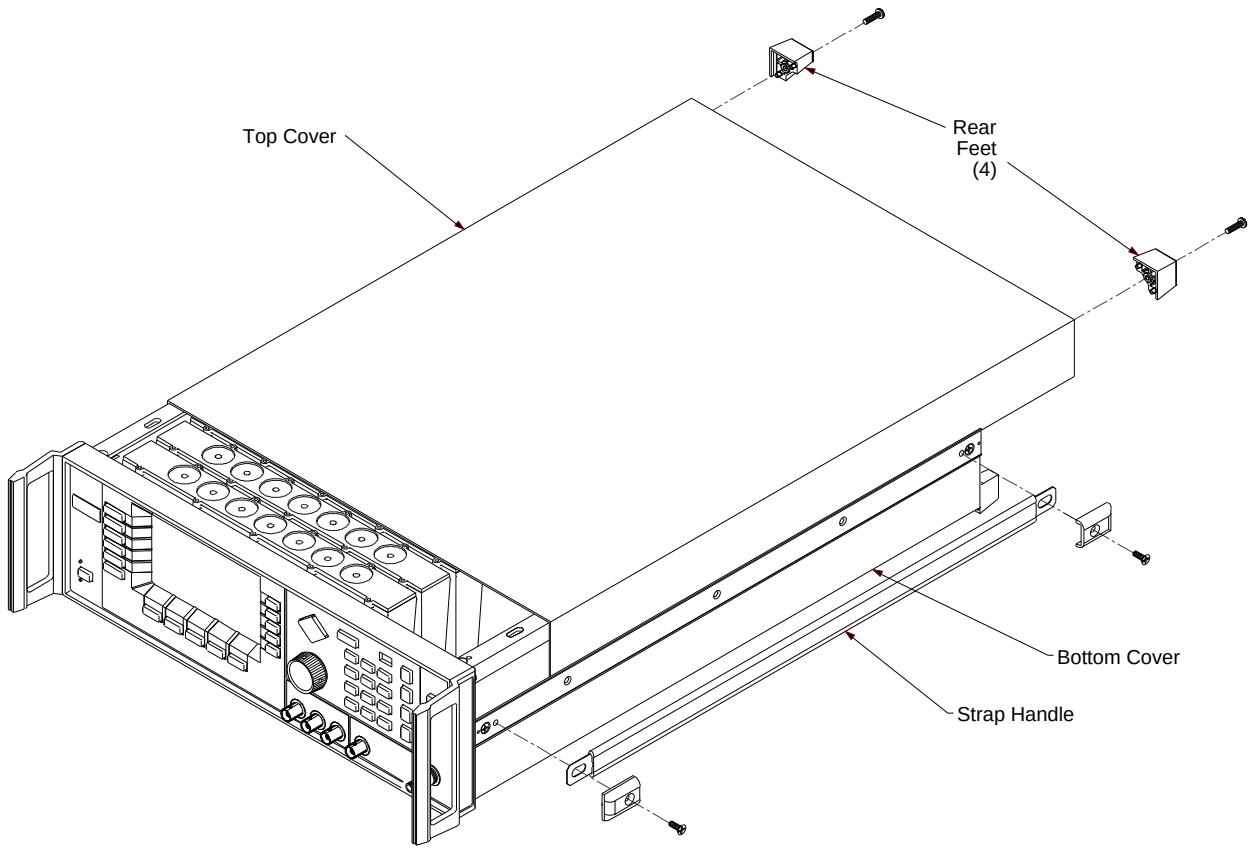


Figure 6-1. *Top Chassis Cover Removal*

6-3 REMOVING AND REPLACING THE FRONT PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the front panel assembly of the 681XXA. The front panel assembly contains the A1 and A2 Front Panel PCBs. Refer to Figure 6-2 during this procedure.

Preliminary Disconnect the power cord from the unit and remove the top and bottom covers as described in paragraph 6-2.

Procedure Remove and replace the front panel assembly as follows:

Step 1 With the instrument in an upright position, remove the two screws from the front of each of the upper rails.

Step 2 Remove the screw and end cap from the front of each of the strap handles (see Figure 6-1).

Step 3 Remove the screw from the front of each of the side rails.

Step 4 Disconnect the ribbon cable at the upper connector on the front panel assembly.

Step 5 Turn the instrument upside down.

Step 6 Remove the two screws from the front of each of the lower rails.

Step 7 Remove the screw connecting the front panel assembly to the chassis pan.

Step 8 Disconnect the ribbon cable at the lower connector on the front panel assembly.

Step 9 Carefully pull the front panel assembly forward until it is clear of the RF OUTPUT connector.

Step 10 Peel away the trim strips from the front handles. (The replacement front panel assembly comes with new trim strips for the handles.)

Step 11 Loosen the screws and remove the front handles from the front panel assembly.

Step 12 To replace the front panel assembly, reverse the removal process.

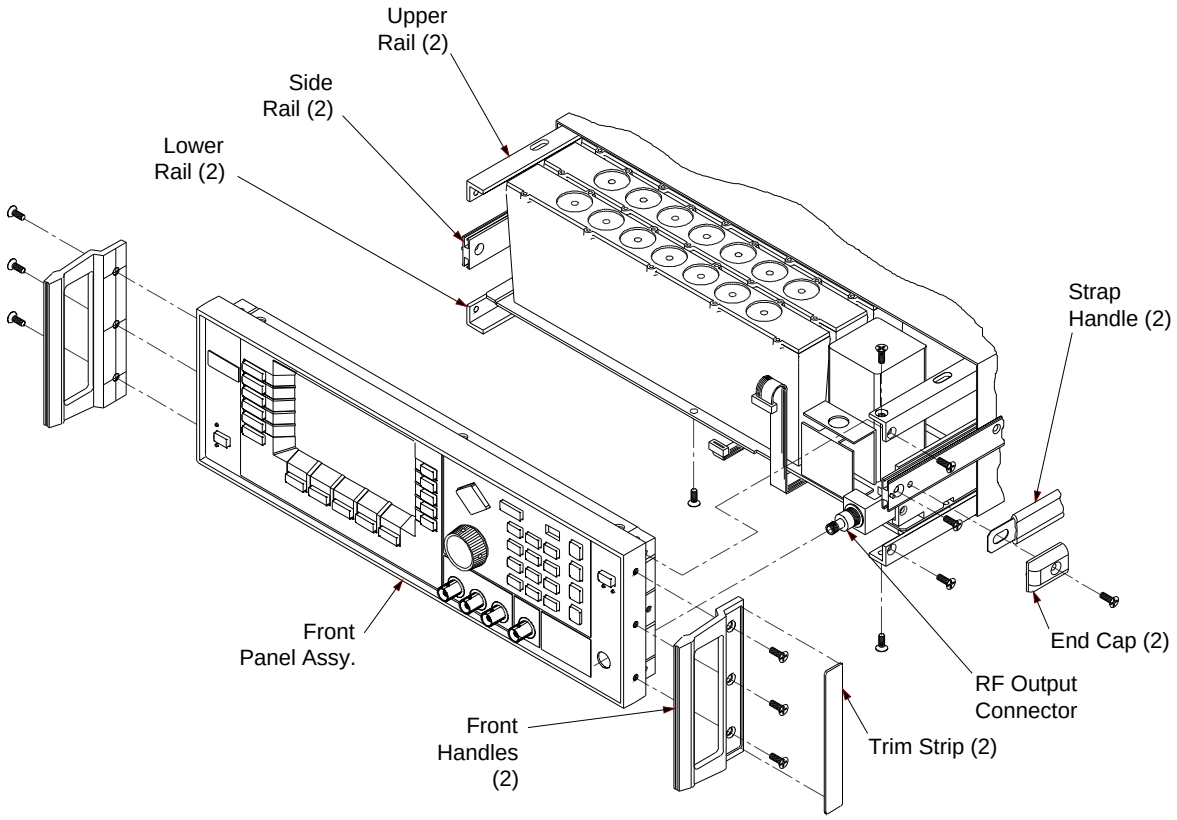


Figure 6-2. *Front Panel Assembly Removal*

6-4 REMOVING AND REPLACING THE A3, A4, A5, OR A6 PCB

This paragraph provides instructions for removing and replacing the A3 Reference Loop PCB, the A4 Coarse Loop PCB, the A5Fine Loop PCB, or the A6 Square Wave Generator PCB, all of which are located in the RF housing (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A3, A4, A5, or A6 PCB as follows:

Step 1 Disconnect the coaxial cables from the PCB to be removed by lifting up on the cable connectors.

Step 2 Using a Phillips screwdriver, remove the nine screws that retain the RF housing cover and set aside.

Step 3 Remove the RF housing cover and set aside.

Step 4 Lift up on the edge tabs of the PCB and lift it out of the RF housing.

Step 5 Remove the “O” rings installed on each MCX connector and retain them for use on the replacement PCB.

Step 6 To replace the PCB, reverse the removal process.

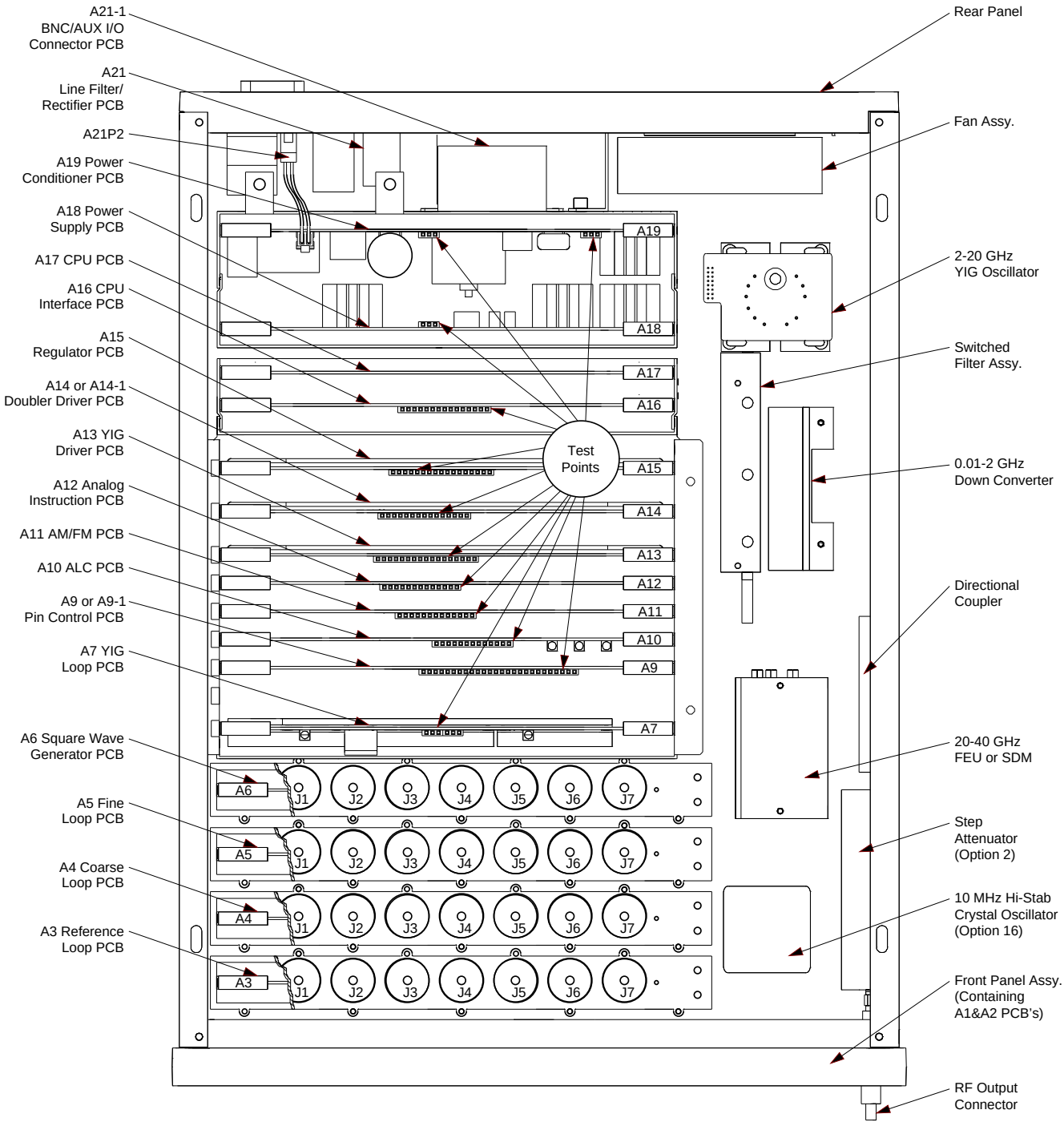


Figure 6-3. *Assembly and Component Locator Diagram*

6-5 REMOVING AND REPLACING THE A7 PCB

This paragraph provides instructions for removing and replacing the A7 YIG Loop PCB, which is located in the main card cage (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A7 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 Using a 5/16-inch wrench, disconnect coaxial cable W2 from the Sampler/SRD module on the PCB.

Step 3 Disconnect the coaxial cables at A7J1 and A7J5 by lifting up on the cable connectors.

Step 4 Lift up on the edge tabs of the PCB and lift it out of the card cage.

Step 5 To replace the A7 PCB, reverse the removal process.

6-6 REMOVING AND REPLACING THE A9, A10, A11, OR A12 PCB

This paragraph provides instructions for removing and replacing the A9/A9-1 PIN Control PCB, the A10 ALC PCB, the A11 AM/FM PCB, or the A12 Analog Instruction PCB, all of which are located in the main card cage (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A9/A9-1, A10, A11, or A12 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 If the A10 PCB is being removed, disconnect the coaxial cable(s) at A10J2 and A10J3 (if used) by lifting up on the cable connector(s).

Step 3 Lift up on the edge tabs of the PCB and lift it out of the card cage..

Step 4 To replace the PCB, reverse the removal process.

6-7 REMOVING AND REPLACING THE A13, A14, OR A15 PCB

This paragraph provides instructions for removing and replacing the A13 YIG Driver PCB, the A14 Doubler Driver/A14-1 SDM Driver PCB, or the A15 Regulator PCB, all of which are located in the main card cage (see Figure 6-3). Each of these PCB assemblies consists of a PCB and a PCB Heat Sink subassembly.

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A13, A14/A14-1, or A15 PCB as follows:

Step 1 Remove the main card cage cover and set aside.

Step 2 Lift up on the edge tabs of the PCB and lift it out of the card cage.

Step 3 Using a Phillips screwdriver, remove the two screws that fasten the PCB Heat Sink subassembly to the chassis pan.

Step 4 Lift the PCB Heat Sink subassembly out of the card cage.

Step 5 To replace the PCB, reverse the removal process.

6-8 REMOVING AND REPLACING THE A16 OR A17 PCB

This paragraph provides instructions for removing and replacing the A16 CPU Interface PCB or the A17 CPU PCB, both of which are located in the CPU housing assembly (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

Procedure Remove and replace the A16 or A17 PCB as follows:

Step 1 Remove the CPU cover and set aside.

Step 2 Lift up on the edge tabs of the PCB and lift it out of the CPU housing.

Step 3 To replace the PCB, reverse the removal process.

6-9 REMOVING AND REPLACING THE A18 OR A19 PCB

This paragraph provides instructions for removing and replacing the A18 Power Supply PCB or the A19 AC Line Conditioner PCB, both of which are located in the power supply housing assembly (see Figure 6-3).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing either the A18 or A19 PCB.

Procedure Remove and replace the A18 or A19 PCB as follows:

Step 1 Remove the power supply cover and set it aside.

Step 2 If the A19 PCB is being removed, disconnect the cable assembly from the A21 Line Filter/Rectifier PCB at A19J2.

Step 3 Lift up the edge tabs on the PCB and lift it out of the power supply housing.

Step 4 To replace the PCB, reverse the removal process.

6-10 REMOVING AND REPLACING THE A21-1 PCB

This paragraph provides instructions for removing and replacing the A21-1 BNC/AUX I/O Connector PCB, which is located on the rear panel assembly (see Figure 6-4).

Preliminary Disconnect the power cord from the unit and remove the top cover as described in paragraph 6-2.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the A21-1 PCB.

Procedure Remove and replace the A21-1 PCB as follows:

Step 1 Using a 7/16-inch wrench, remove the coaxial cables going to the rear panel 10 MHz REF IN and 10 MHz REF OUT BNC connectors.

Step 2 Remove the plastic high voltage safety shield located over the A21 Line Filter/Rectifier PCB.

Step 3 Disconnect the fan cable connector from J13 on the Motherboard.

Step 4 Disconnect the ribbon cable connector from the A21-1 PCB.

Step 5 Using a WILTRON P/N T1451 tool, remove the dress nuts from the 11 rear panel BNC connectors.

Step 6 Carefully remove the A21-1 PCB from the rear panel assembly.

Step 7 To replace the PCB, reverse the removal process.

6-11 REMOVING AND REPLACING THE REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the rear panel assembly of the 681XXA. The rear panel assembly contains the A21 Line Filter/Rectifier PCB, the A21-1 BNC/AUX I/O Connector PCB, the line module assembly, and the fan assembly. Refer to Figure 6-4 during this procedure.

Preliminary Disconnect the power cord from the unit and remove the top and bottom covers as described in paragraph 6-2.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the rear panel assembly as follows:

Step 1 Remove the four screws that fasten the rear panel overlay to the rear panel assembly and set aside.

Step 2 Remove the rear panel overlay and set aside.

Step 3 Turn the instrument upside down.

Step 4 Remove the two screws from the rear of each of the lower rails and set aside.

Step 5 Return the instrument to the upright position.

Step 6 Remove the two screws from the rear of each of the upper rails and set aside.

Step 7 Remove the screw and end cap from the rear of each of the strap handles and set aside (see Figure 6-1).

Step 8 Remove the screw from the rear of each of the side rails and set aside.

Step 9 Loosen the two screws that fasten the rear panel assembly to the power supply housing. (These screws are accessable via holes above and below the AUX I/O connector on the rear panel.)

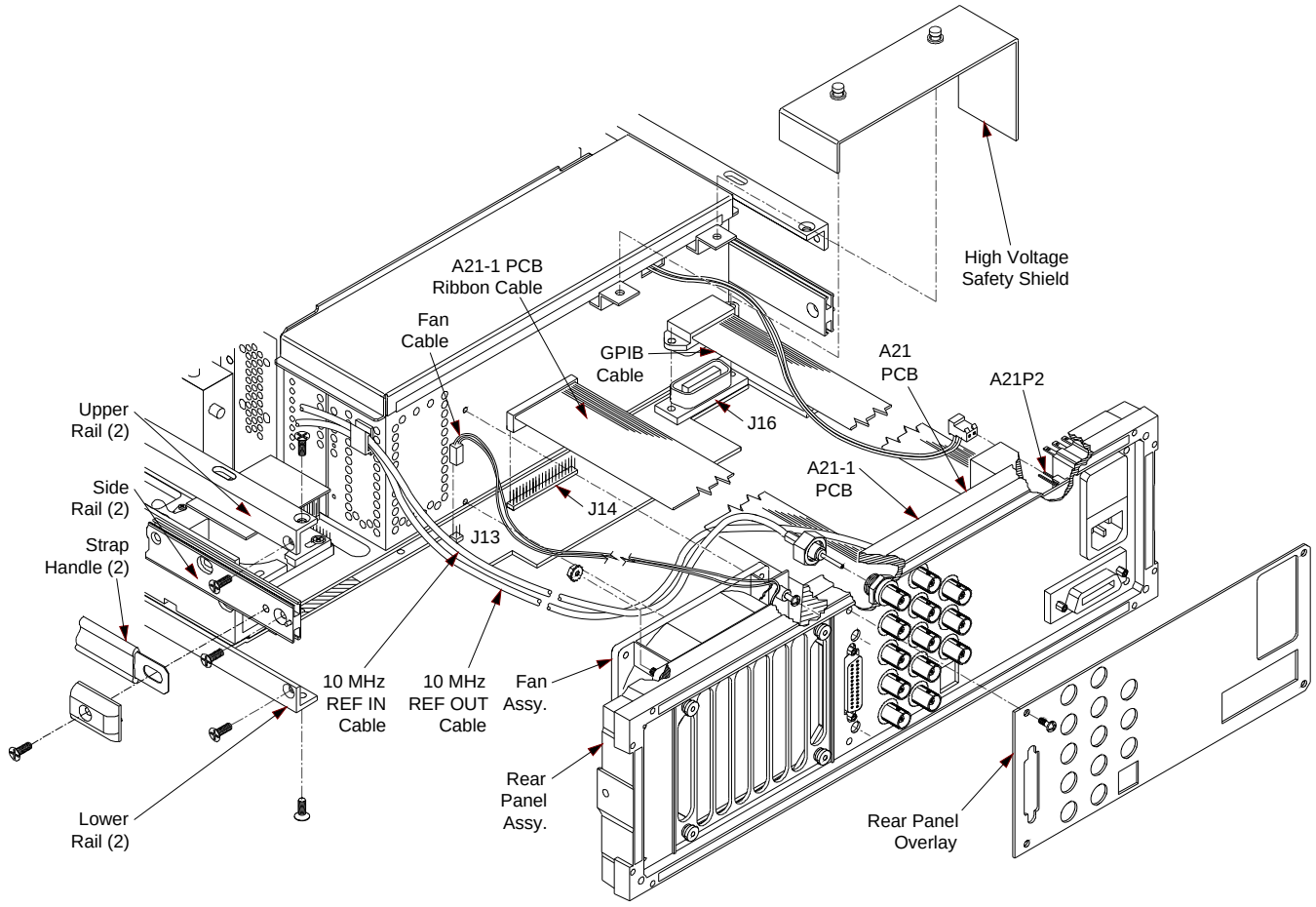


Figure 6-4. *Rear Panel Assembly Removal*

Step 10 Using a 7/16-inch wrench, disconnect the coaxial cables going to the rear panel 10 MHz REF IN and 10 MHz REF OUT BNC connectors.

Step 11 Remove the plastic high voltage safety shield located over the A21 Line Filter/Rectifier PCB.

Step 12 Disconnect the cable from connector P2 on the A21 PCB.

Step 13 Carefully pull the rear panel assembly away from the 681XXA chassis until the cable connections to the Motherboard are accessable.

Step 14 Disconnect the fan cable connector from J13 on the Motherboard.

Step 15 Disconnect the A21-1 PCB ribbon cable connector from J14 on the Motherboard.

Step 16 Disconnect the GPIB cable connector from J16 on the Motherboard.

Step 17 Carefully pull the rear panel assembly completely free from the 681XXA chassis.

Step 18 To replace the rear panel assembly, reverse the removal process.

6-12 REMOVING AND REPLACING THE A21 PCB

This paragraph provides instructions for removing and replacing the A21 Line Filter/Rectifier PCB, which is located on the rear panel assembly (see Figure 6-4).

Preliminary Disconnect the power cord from the unit. Remove the top and bottom covers as described in paragraph 6-2. Remove the rear panel assembly as described in paragraph 6-11.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the A21 PCB as follows:

Step 1 Disconnect the cables connected to P1, P2, and P6 on the PCB.

Step 2 Remove the four screw that fasten the PCB to the rear panel assembly and set aside.

Step 3 Remove the PCB from the rear panel assembly.

Step 4 To replace the PCB, reverse the removal process.

6-13 REMOVING AND REPLACING THE FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the fan assembly, which is located on the rear panel assembly (see Figure 6-4).

Preliminary Disconnect the power cord from the unit. Remove the top and bottom covers as described in paragraph 6-2. Remove the rear panel assembly as described in paragraph 6-11.

WARNING

When power is removed from the instrument, ***always*** allow five minutes for the capacitors on the A21 Line Filter/Rectifier PCB to discharge before removing the rear panel assembly.

Procedure Remove and replace the fan assembly as follows:

Step 1 With the rear panel laying flat, use a ¼-inch wrench to remove the four kep nuts and flat washers that fasten the fan assembly to the rear panel.

Step 2 Lift the fan assembly from the rear panel assembly.

Step 3 Clean the honeycomb fan filter as required before replacing the fan assembly.

Step 4 To replace the fan assembly, reverse the removal process.

NOTE

To ensure proper cooling of the unit, ***always*** mount the fan assembly with the airflow direction indicator arrow on the fan body pointing toward the interior of the instrument.

Appendix A
Test Records

A-1 INTRODUCTION

This appendix provides test records for recording the results of the Performance Verification tests (Chapter 3) and the Calibration procedures (Chapter 4). They jointly provide the means for maintaining an accurate and complete record of instrument performance. Test records are provided for all four models of the Series 681XXA Synthesized Sweep Generator.

Each test record has been customized to cover a particular sweep generator model. It contains specific references to frequency parameters and power levels that are applicable only to that instrument model and its available options.

We recommend that you make a copy of these pages each time the test procedures are performed. By dating each Test Record copy, a detailed history of instrument performance can be accumulated.

WILTRON Model 68137A **Date:** _____

Serial Number _____ **Tested By:** _____

3-5. Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record T_S value	_____hours	
Record T_1 value	_____sec	
Record T_2 value	_____sec	
Record T_F value	_____hours	
Record the calculated aging rate	_____per day	$1x10^{-7}$ per day ($5x10^{-10}$ per day with Option 16)

3-6. Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *
2.000 000 000	_____
3.000 000 000	_____
4.000 000 000	_____
5.000 000 000	_____
6.000 000 000	_____
7.000 000 000	_____
8.000 000 000	_____
9.000 000 000	_____
10.000 000 000	_____
11.000 000 000	_____
12.000 000 000	_____
13.000 000 000	_____
14.000 000 000	_____
15.000 000 000	_____
16.000 000 000	_____
17.000 000 000	_____
18.000 000 000	_____
19.000 000 000	_____
20.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (Standard 68137A)

Test Frequency (in GHz)	Measured Value **
2.000 001 000	_____
2.000 002 000	_____
2.000 003 000	_____
2.000 004 000	_____
2.000 005 000	_____
2.000 006 000	_____
2.000 007 000	_____
2.000 008 000	_____
2.000 009 000	_____
2.000 010 000	_____

** Specification for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (68137A with Option 11)

Test Frequency (in GHz)	Measured Value ***
2.000 000 100	_____
2.000 000 200	_____
2.000 000 300	_____
2.000 000 400	_____
2.000 000 500	_____
2.000 000 600	_____
2.000 000 700	_____
2.000 000 800	_____
2.000 000 900	_____
2.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz

3-7. Spurious Signals Test: RF Output Signals <2 GHz

This test is not applicable to the 68137A model.

3.8 Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.1 GHz		
Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz		
Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz		
Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz		
Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15 (High Power) installed.

3.8 Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz		
Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz		
Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz		
Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15 (High Power) installed.

3-9. Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 5.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–67 dBc
1 kHz	_____dBc	–75 dBc
10 kHz	_____dBc	–83 dBc
100 kHz	_____dBc	–87 dBc
Set F1 to 15.0 GHz		
Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–58 dBc
1 kHz	_____dBc	–71 dBc
10 kHz	_____dBc	–73 dBc
100 kHz	_____dBc	–82 dBc

3-10. Power Level Accuracy and Flatness Tests (68137A Models without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	Measured Power *
+13.0 dBm	_____dBm
+12.0 dBm	_____dBm
+11.0 dBm	_____dBm
+10.0 dBm	_____dBm
+ 9.0 dBm	_____dBm
+ 8.0 dBm	_____dBm
+ 7.0 dBm	_____dBm
+ 6.0 dBm	_____dBm
+ 5.0 dBm	_____dBm
+ 4.0 dBm	_____dBm
+ 3.0 dBm	_____dBm
+ 2.0 dBm	_____dBm
+ 1.0 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+13.0 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure(Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+13.0 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68137A Models with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	Measured Power *
+10.0 dBm	_____dBm
+ 9.0 dBm	_____dBm
+ 8.0 dBm	_____dBm
+ 7.0 dBm	_____dBm
+ 6.0 dBm	_____dBm
+ 5.0 dBm	_____dBm
+ 4.0 dBm	_____dBm
+ 3.0 dBm	_____dBm
+ 2.0 dBm	_____dBm
+ 1.0 dBm	_____dBm
+ 0.0 dBm	_____dBm
– 1.0 dBm	_____dBm
– 2.0 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+10.0 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+10.0 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68137A Models with Option 15 High Power and without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	Measured Power *
+17.0 dBm	_____dBm
+16.0 dBm	_____dBm
+15.0 dBm	_____dBm
+14.0 dBm	_____dBm
+13.0 dBm	_____dBm
+12.0 dBm	_____dBm
+11.0 dBm	_____dBm
+10.0 dBm	_____dBm
+ 9.0 dBm	_____dBm
+ 8.0 dBm	_____dBm
+ 7.0 dBm	_____dBm
+ 6.0 dBm	_____dBm
+ 5.0 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+17.0 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+17.0 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68137A Models with Option 15 High Power and Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz

Set L1 to:	Measured Power *
+14.0 dBm	_____dBm
+13.0 dBm	_____dBm
+12.0 dBm	_____dBm
+11.0 dBm	_____dBm
+10.0 dBm	_____dBm
+ 9.0 dBm	_____dBm
+ 8.0 dBm	_____dBm
+ 7.0 dBm	_____dBm
+ 6.0 dBm	_____dBm
+ 5.0 dBm	_____dBm
+ 4.0 dBm	_____dBm
+ 3.0 dBm	_____dBm
+ 2.0 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+14.0 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+14.0 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

WILTRON Model 68137A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7. Preliminary Calibration

Procedure Step	**Step Completion**
Reset the Linearizer DACs	_____
1. Internal DVM Calibration (calterm119)	_____
2. Coarse Loop Pretune DAC Calibration (calterm 137)	_____
3. Fine Loop Pretune DAC Calibration (calterm 136)	_____
4. Sweep Time DAC Calibration (calterm 132)	_____
5. Center Frequency DAC Calibration (calterm 114)	_____
6. YIG Frequency Offset DAC Calibration (calterm 134)	_____
7. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
8. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
9. FM Coil Sensitivity Calibration DAC Calibration (calterm 135)	_____
10. Sweep Width DAC Calibration (calterm 133)	_____
11. FEU Input Power Levels Calibration (calterm 140) (*This step is not applicable to the 68137A*)	N/A
12. Store the Calibration Data	_____

4-8. Switched Filter Shaper Calibration

Minimum Unleveled Power Point Measurement **Measured Frequency**

5. Record the minimum unleveled power point frequency for each frequency band:
   - Band 1 (2.0-3.3 GHz) . . . . . _____GHz
   - Band 2 (3.3-5.5 GHz) . . . . . _____GHz
   - Band 3 (5.5-8.4 GHz) . . . . . _____GHz
   - Band 4 (8.4-13.25 GHz) . . . . . _____GHz
   - Band 5 (13.25-20.0 GHz) . . . . . _____GHz

Shaper DAC Adjustment **DAC Setting Value**

4.c Record the DAC's setting value for each frequency band:
   - Band 1 (2.0-3.3 GHz) . . . . . _____
   - Band 2 (3.3-5.5 GHz) . . . . . _____
   - Band 3 (5.5-8.4 GHz) . . . . . _____
   - Band 4 (8.4-13.25 GHz) . . . . . _____
   - Band 5 (13.25-20.0 GHz) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):
   - Select Item 4 for Band 1 (2.0-3.3 GHz) . . . . . _____
   - Select Item 5 for Band 2 (3.3-5.5 GHz) . . . . . _____
   - Select Item 6 for Band 3 (5.5-8.4 GHz) . . . . . _____
   - Select Item 7 for Band 4 (8.4-13.25 GHz) . . . . . _____
   - Select Item 8 for Band 5 (13.25-20.0 GHz) . . . . . _____

Store DAC Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-9. ALC Slope Calibration

Procedure Step	**Step Completion**
5. ALC Slope DAC adjustment for ≤2 GHz (*This step is not applicable to the 68137A*)	N/A
9. ALC Slope DAC adjustment for >2 GHz	
10. Store the DAC setting value(s)	

4-10. RF Level Calibration

This calibration is performed using an automatic test system. Contact AWSC Customer Service for further information.

4-11. AM Bandwidth Calibration

AM Bandwidth Adjustment	**DAC Setting Value**
5.c Record the DAC's setting value for each frequency band:	
Band 1 (2.0-3.3 GHz)	
Band 2 (3.3-5.5 GHz)	
Band 3 (5.5-8.4 GHz)	
Band 4 (8.4-13.25 GHz)	
Band 5 (13.25-20.0 GHz)	

Enter DAC Settings	**Step Completion**
1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):	
Select Item 22 for Band 1 (2.0-3.3 GHz)	
Select Item 23 for Band 2 (3.3-5.5 GHz)	
Select Item 24 for Band 3 (5.5-8.4 GHz)	
Select Item 25 for Band 4 (8.4-13.25 GHz)	
Select Item 26 for Band 5 (13.25-20.0 GHz)	

Store Dac Settings	**Step Completion**
1. Store the DAC setting values	

4-12. AM Calibration

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. Store the Calibration Data	_____

4-13. FM Calibration

Procedure Step	Step Completion
2. FM Meter Calibration (calterm 123)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. Store the Calibration Data	_____

WILTRON Model 68147A **Date:** _____

Serial Number _____ **Tested By:** _____

3-5. Internal Time Base Aging Rate Test

Test Procedure	**Measured Value**	**Upper Limit**
Record T_S value	_____hours	
Record T_1 value	_____sec	
Record T_2 value	_____sec	
Record T_F value	_____hours	
Record the calculated aging rate	_____per day	$1x10^{-7}$ per day ($5x10^{-10}$ per day with Option 16)

3-6. Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____
2.000 000 000	_____
3.000 000 000	_____
4.000 000 000	_____
5.000 000 000	_____
6.000 000 000	_____
7.000 000 000	_____
8.000 000 000	_____
9.000 000 000	_____
10.000 000 000	_____
11.000 000 000	_____
12.000 000 000	_____
13.000 000 000	_____
14.000 000 000	_____
15.000 000 000	_____
16.000 000 000	_____
17.000 000 000	_____
18.000 000 000	_____
19.000 000 000	_____
20.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (Standard 68147A)

Test Frequency (in GHz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz

Fine Loop Test Procedure (68147A with Option 11)

Test Frequency (in GHz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-7. Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz		
Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz		
Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz		
Record the level of the harmonics of the 1.6 GHz carrier:		
3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-8. Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measured Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc*
8.4 GHz (4th harmonic)	_____dBc	–60 dBc*
10.5 GHz (5th harmonic)	_____dBc	–60 dBc*
12.6 GHz (6th harmonic)	_____dBc	–60 dBc*
14.7 GHz (7th harmonic)	_____dBc	–60 dBc*
16.8 GHz (8th harmonic)	_____dBc	–60 dBc*
18.9 GHz (9th harmonic)	_____dBc	–60 dBc*
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc*
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc*
14.4 GHz (4th harmonic)	_____dBc	–60 dBc*
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc*
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15 (High Power) installed.

3-8. Harmonic Test: RF Output Signals From 2 to 20 GHz (Continued)

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc*
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc*
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc*
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc*

* –50 dBc if Option 15 (High Power) installed.

3-9. Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 5.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–67 dBc
1 kHz	_____dBc	–75 dBc
10 kHz	_____dBc	–83 dBc
100 kHz	_____dBc	–87 dBc
Set F1 to 15.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–58 dBc
1 kHz	_____dBc	–71 dBc
10 kHz	_____dBc	–73 dBc
100 kHz	_____dBc	–82 dBc

3-10. Power Level Accuracy and Flatness Tests (68147A Models without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+13 dBm	_____dBm
+12 dBm	_____dBm	+12 dBm	_____dBm
+11 dBm	_____dBm	+11 dBm	_____dBm
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+13 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+13 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68147A Models with Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+10 dBm	_____dBm	+10 dBm	_____dBm
+ 9 dBm	_____dBm	+ 9 dBm	_____dBm
+ 8 dBm	_____dBm	+ 8 dBm	_____dBm
+ 7 dBm	_____dBm	+ 7 dBm	_____dBm
+ 6 dBm	_____dBm	+ 6 dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm
– 2 dBm	_____dBm	– 2 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+10 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+10 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68147A Models with Option 15 High Power and without Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+13 dBm	_____dBm	+17 dBm	_____dBm
+12 dBm	_____dBm	+16 dBm	_____dBm
+11 dBm	_____dBm	+15 dBm	_____dBm
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+ 12dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+17 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+17 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68147A Models with Option 15 High Power and Option 2A Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power**
+10 dBm	_____dBm	+14 dBm	_____dBm
+ 9 dBm	_____dBm	+13 dBm	_____dBm
+ 8 dBm	_____dBm	+12 dBm	_____dBm
+ 7 dBm	_____dBm	+11 dBm	_____dBm
+ 6 dBm	_____dBm	+10 dBm	_____dBm
+ 5 dBm	_____dBm	+ 9 dBm	_____dBm
+ 4 dBm	_____dBm	+ 8 dBm	_____dBm
+ 3 dBm	_____dBm	+ 7 dBm	_____dBm
+ 2 dBm	_____dBm	+ 6 dBm	_____dBm
+ 1 dBm	_____dBm	+ 5 dBm	_____dBm
+ 0 dBm	_____dBm	+ 4 dBm	_____dBm
– 1 dBm	_____dBm	+ 3 dBm	_____dBm
– 2 dBm	_____dBm	+ 2 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+14 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+14 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (typical, not a specification).

WILTRON Model 68147A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7. Preliminary Calibration

Procedure Step	**Step Completion**
Reset the Linearizer DACs	_____
1. Internal DVM Calibration (calterm119)	_____
2. Coarse Loop Pretune DAC Calibration (calterm 137)	_____
3. Fine Loop Pretune DAC Calibration (calterm 136)	_____
4. Sweep Time DAC Calibration (calterm 132)	_____
5. Center Frequency DAC Calibration (calterm 114)	_____
6. YIG Frequency Offset DAC Calibration (calterm 134)	_____
7. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
8. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
9. FM Coil Sensitivity Calibration DAC Calibration (calterm 135)	_____
10. Sweep Width DAC Calibration (calterm 133)	_____
11. FEU Input Power Levels Calibration (calterm 140) (*This step is not applicable to the 68147A*)	N/A
12. Store the Calibration Data	_____

4-8. Switched Filter Shaper Calibration

Minimum Unleveled Power Point Measurement **Measured Frequency**

5. Record the minimum unleveled power point frequency for each frequency band:
   - Band 0 (0.01-2.0 GHz) . . . . . _____GHz
   - Band 1 (2.0-3.3 GHz) . . . . . _____GHz
   - Band 2 (3.3-5.5 GHz) . . . . . _____GHz
   - Band 3 (5.5-8.4 GHz) . . . . . _____GHz
   - Band 4 (8.4-13.25 GHz) . . . . . _____GHz
   - Band 5 (13.25-20.0 GHz) . . . . . _____GHz

Shaper DAC Adjustment **DAC Setting Value**

4.c Record the DAC's setting value for each frequency band:
   - Band 0 (0.01-2.0 GHz) . . . . . _____
   - Band 1 (2.0-3.3 GHz) . . . . . _____
   - Band 2 (3.3-5.5 GHz) . . . . . _____
   - Band 3 (5.5-8.4 GHz) . . . . . _____
   - Band 4 (8.4-13.25 GHz) . . . . . _____
   - Band 5 (13.25-20.0 GHz) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):
   - Select Item 3 for Band 0 (0.01-2.0 GHz) . . . . . _____
   - Select Item 4 for Band 1 (2.0-3.3 GHz) . . . . . _____
   - Select Item 5 for Band 2 (3.3-5.5 GHz) . . . . . _____
   - Select Item 6 for Band 3 (5.5-8.4 GHz) . . . . . _____
   - Select Item 7 for Band 4 (8.4-13.25 GHz) . . . . . _____
   - Select Item 8 for Band 5 (13.25-20.0 GHz) . . . . . _____

Store DAC Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-9. ALC Slope Calibration

Procedure Step	Step Completion
5. ALC Slope DAC adjustment for ≤2 GHz	_____
9. ALC Slope DAC adjustment for >2 GHz	_____
10. Store the DAC setting value(s)	_____

4-10. RF Level Calibration

This calibration is performed using an automatic test system. Contact AWSC Customer Service for further information.

4-11. AM Bandwidth Calibration

AM Bandwidth Adjustment	DAC Setting Value
5.c Record the DAC's setting value for each frequency band:	
Band 0 (0.01-2.0 GHz)	_____
Band 1 (2.0-3.3 GHz)	_____
Band 2 (3.3-5.5 GHz)	_____
Band 3 (5.5-8.4 GHz)	_____
Band 4 (8.4-13.25 GHz)	_____
Band 5 (13.25-20.0 GHz)	_____

Enter DAC Settings	Step Completion
1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):	
Select Item 21 for Band 0 (0.01-2.0 GHz)	_____
Select Item 22 for Band 1 (2.0-3.3 GHz)	_____
Select Item 23 for Band 2 (3.3-5.5 GHz)	_____
Select Item 24 for Band 3 (5.5-8.4 GHz)	_____
Select Item 25 for Band 4 (8.4-13.25 GHz)	_____
Select Item 26 for Band 5 (13.25-20.0 GHz)	_____

Store Dac Settings	Step Completion
1. Store the DAC setting values	_____

4-12. AM Calibration

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. Store the Calibration Data	_____

4-13. FM Calibration

Procedure Step	Step Completion
2. FM Meter Calibration (calterm 123)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. Store the Calibration Data	_____

WILTRON Model 68163A **Date:** _____

Serial Number _____ **Tested By:** _____

3-5. Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record T_S value	_____hours	
Record T_1 value	_____sec	
Record T_2 value	_____sec	
Record T_F value	_____hours	
Record the calculated aging rate	_____per day	$1x10^{-7}$ per day ($5x10^{-10}$ per day with Option 16)

3-6. Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
2.000 000 000	_____	21.000 000 000	_____
3.000 000 000	_____	22.000 000 000	_____
4.000 000 000	_____	23.000 000 000	_____
5.000 000 000	_____	24.000 000 000	_____
6.000 000 000	_____	25.000 000 000	_____
7.000 000 000	_____	26.000 000 000	_____
8.000 000 000	_____	27.000 000 000	_____
9.000 000 000	_____	28.000 000 000	_____
10.000 000 000	_____	29.000 000 000	_____
11.000 000 000	_____	30.000 000 000	_____
12.000 000 000	_____	31.000 000 000	_____
13.000 000 000	_____	32.000 000 000	_____
14.000 000 000	_____	33.000 000 000	_____
15.000 000 000	_____	34.000 000 000	_____
16.000 000 000	_____	35.000 000 000	_____
17.000 000 000	_____	36.000 000 000	_____
18.000 000 000	_____	37.000 000 000	_____
19.000 000 000	_____	38.000 000 000	_____
20.000 000 000	_____	39.000 000 000	_____
		40.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-6. Frequency Synthesis Tests

Fine Loop Test Procedure (Standard 68163A)

Test Frequency (in GHz)	Measured Value **
2.000 001 000	_____
2.000 002 000	_____
2.000 003 000	_____
2.000 004 000	_____
2.000 005 000	_____
2.000 006 000	_____
2.000 007 000	_____
2.000 008 000	_____
2.000 009 000	_____
2.000 010 000	_____

** Specification for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (68163A with Option 11)

Test Frequency (in GHz)	Measured Value ***
2.000 000 100	_____
2.000 000 200	_____
2.000 000 300	_____
2.000 000 400	_____
2.000 000 500	_____
2.000 000 600	_____
2.000 000 700	_____
2.000 000 800	_____
2.000 000 900	_____
2.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-7. Spurious Signals Test: RF Output Signals <2 GHz

This test is not applicable to the 68163A model.

3-8. Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	Measured Value	Upper Limit
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc
8.4 GHz (4th harmonic)	_____dBc	–60 dBc
10.5 GHz (5th harmonic)	_____dBc	–60 dBc
12.6 GHz (6th harmonic)	_____dBc	–60 dBc
14.7 GHz (7th harmonic)	_____dBc	–60 dBc
16.8 GHz (8th harmonic)	_____dBc	–60 dBc
18.9 GHz (9th harmonic)	_____dBc	–60 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc
14.4 GHz (4th harmonic)	_____dBc	–60 dBc
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc

Test Procedure (11 to 20 GHz)	Measured Value	Upper Limit
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc

3-9. Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 5.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–67 dBc
1 kHz	_____dBc	–75 dBc
10 kHz	_____dBc	–83 dBc
100 kHz	_____dBc	–87 dBc
Set F1 to 15.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–58 dBc
1 kHz	_____dBc	–71 dBc
10 kHz	_____dBc	–73 dBc
100 kHz	_____dBc	–82 dBc
Set F1 to 26.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–52 dBc
1 kHz	_____dBc	–65 dBc
10 kHz	_____dBc	–67 dBc
100 kHz	_____dBc	–76 dBc

3-10. Power Level Accuracy and Flatness Tests (68163A Models without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 26.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 6dBm	_____dBm	+ 6dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2dBm	_____dBm	+ 2dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm
– 2 dBm	_____dBm	– 2 dBm	_____dBm
– 3 dBm	_____dBm	– 3 dBm	_____dBm
– 4 dBm	_____dBm	– 4 dBm	_____dBm
– 5 dBm	_____dBm	– 5 dBm	_____dBm
– 6 dBm	_____dBm	– 6 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

3-10. Power Level Accuracy and Flatness Tests (68163A Models with Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 5.0 GHz		Set F1 to 26.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm
– 2 dBm	_____dBm	– 2 dBm	_____dBm
– 3 dBm	_____dBm	– 3 dBm	_____dBm
– 4 dBm	_____dBm	– 4 dBm	_____dBm
– 5 dBm	_____dBm	– 5 dBm	_____dBm
– 6 dBm	_____dBm	– 6 dBm	_____dBm
– 7 dBm	_____dBm	– 7 dBm	_____dBm
– 8 dBm	_____dBm	– 8 dBm	_____dBm
– 9 dBm	_____dBm	– 9 dBm	_____dBm
–10 dBm	_____dBm	–10 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation ****
+ 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	**Max Power**	**Min Power**	**Variation *****
+ 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (2 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

WILTRON Model 68163A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7. Preliminary Calibration

Procedure Step	**Step Completion**
Reset the Linearizer DACs	_____
1. Internal DVM Calibration (calterm119)	_____
2. Coarse Loop Pretune DAC Calibration (calterm 137)	_____
3. Fine Loop Pretune DAC Calibration (calterm 136)	_____
4. Sweep Time DAC Calibration (calterm 132)	_____
5. Center Frequency DAC Calibration (calterm 114)	_____
6. YIG Frequency Offset DAC Calibration (calterm 134)	_____
7. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
8. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
9. FM Coil Sensitivity Calibration DAC Calibration (calterm 135)	_____
10. Sweep Width DAC Calibration (calterm 133)	_____
11. FEU Input Power Levels Calibration (calterm 140) (*This step only applies to units that contain a FEU; i.e., Models 68163A that have serial numbers below 320001*)	_____
12. Store the Calibration Data	_____

4-8. Switched Filter Shaper Calibration

Minimum Unleveled Power Point Measurement **Measured Frequency**

5. Record the minimum unleveled power point frequency for each frequency band:
   - Band 1 (2.0-3.3 GHz) . . . . . _____GHz
   - Band 2 (3.3-5.5 GHz) . . . . . _____GHz
   - Band 3 (5.5-8.4 GHz) . . . . . _____GHz
   - Band 4 (8.4-13.25 GHz) . . . . . _____GHz
   - Band 5 (13.25-20.0 GHz) . . . . . _____GHz

   The following applies only to units containing a FEU:
   - Band 6 (20.0-26.5 GHz) . . . . . _____GHz
   - Band 7 (26.5-33.0 GHz) . . . . . _____GHz
   - Band 8 (33.0-40.0 GHz) . . . . . _____GHz

Shaper DAC Adjustment **DAC Setting Value**

4.c Record the DAC's setting value for each frequency band:
   - Band 1 (2.0-3.3 GHz) . . . . . _____
   - Band 2 (3.3-5.5 GHz) . . . . . _____
   - Band 3 (5.5-8.4 GHz) . . . . . _____
   - Band 4 (8.4-13.25 GHz) . . . . . _____
   - Band 5 (13.25-20.0 GHz) _____

9.c *The following applies only to units containing a FEU:*
   - Band 6 (20.0-26.5 GHz) . . . . . _____
   - Band 7 (26.5-33.0 GHz) . . . . . _____
   - Band 8 (33.0-40.0 GHz) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):
   - Select Item 4 for Band 1 (2.0-3.3 GHz) . . . . . _____
   - Select Item 5 for Band 2 (3.3-5.5 GHz) . . . . . _____
   - Select Item 6 for Band 3 (5.5-8.4 GHz) . . . . . _____
   - Select Item 7 for Band 4 (8.4-13.25 GHz) . . . . . _____
   - Select Item 8 for Band 5 (13.25-20.0 GHz) . . . . . _____

4-8. Switched Filter Shaper Calibration (Continued)

Enter DAC Settings (Continued) **Step Completion**

1.b *The following applies only to units containing a FEU:*
Select Item 9 for Band 6 (20.0-26.5 GHz) . . . . . _____

Select Item 10 for Band 7 (26.5-33.0 GHz) . . . . . _____

Select Item 11 for Band 8 (33.0-40.0 GHz) . . . . . _____

Store DAC Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-9. ALC Slope Calibration

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment for ≤2 GHz
(*This step is not applicable to the 68163A*) . . . . . N/A

9. ALC Slope DAC adjustment for >2 GHz . . . . . _____

10. Store the DAC setting value(s) . . . . . _____

4-10. RF Level Calibration

This calibration is performed using an automatic test system. Contact AWSC Customer Service for further information.

4-11. AM Bandwidth Calibration

AM Bandwidth Adjustment **DAC Setting Value**

5.c Record the DAC's setting value for each frequency band:

Band 1 (2.0-3.3 GHz) . . . . . _____

Band 2 (3.3-5.5 GHz) . . . . . _____

Band 3 (5.5-8.4 GHz) . . . . . _____

Band 4 (8.4-13.25 GHz) . . . . . _____

Band 5 (13.25-20.0 GHz) . . . . . _____

Band 6 (20.0-26.5 GHz w/FEU)/(20.0-25.0 GHz w/SDM) . . . . . _____

Band 7 (26.5-33.0 GHz w/FEU)/(25.0-32.0 GHz w/SDM) . . . . . _____

Band 8 (33.0-40.0 GHz w/FEU)/(32.0-40.0 GHz w/SDM) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):

Select Item 22 for Band 1 (2.0-3.3 GHz) . . . . . _____

Select Item 23 for Band 2 (3.3-5.5 GHz) . . . . . _____

Select Item 24 for Band 3 (5.5-8.4 GHz) . . . . . _____

Select Item 25 for Band 4 (8.4-13.25 GHz) . . . . . _____

Select Item 26 for Band 5 (13.25-20.0 GHz) . . . . . _____

Select Item 27 for Band 6 (20.0-26.5 GHz w/FEU)/(20.0-25.0 GHz w/SDM) . . . . . _____

Select Item 28 for Band 7 (26.5-33.0 GHz w/FEU)/(25.0-32.0 GHz w/SDM) . . . . . _____

Select Item 29 for Band 8 (33.0-40.0 GHz w/FEU)/(32.0-40.0 GHz w/SDM) . . . . . _____

Store Dac Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-12. AM Calibration

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. Store the Calibration Data	_____

4-13. FM Calibration

Procedure Step	Step Completion
2. FM Meter Calibration (calterm 123)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. Store the Calibration Data	_____

WILTRON Model 68169A **Date:** _____

Serial Number _____ **Tested By:** _____

3-5. Internal Time Base Aging Rate Test

Test Procedure	Measured Value	Upper Limit
Record T_S value	_____hours	
Record T_1 value	_____sec	
Record T_2 value	_____sec	
Record T_F value	_____hours	
Record the calculated aging rate	_____per day	$1x10^{-7}$ per day ($5x10^{-10}$ per day with Option 16)

3-6. Frequency Synthesis Tests

Coarse Loop/YIG Loop Test Procedure

Test Frequency (in GHz)	Measured Value *	Test Frequency (in GHz)	Measured Value *
1.000 000 000	_____	21.000 000 000	_____
2.000 000 000	_____	22.000 000 000	_____
3.000 000 000	_____	23.000 000 000	_____
4.000 000 000	_____	24.000 000 000	_____
5.000 000 000	_____	25.000 000 000	_____
6.000 000 000	_____	26.000 000 000	_____
7.000 000 000	_____	27.000 000 000	_____
8.000 000 000	_____	28.000 000 000	_____
9.000 000 000	_____	29.000 000 000	_____
10.000 000 000	_____	30.000 000 000	_____
11.000 000 000	_____	31.000 000 000	_____
12.000 000 000	_____	32.000 000 000	_____
13.000 000 000	_____	33.000 000 000	_____
14.000 000 000	_____	34.000 000 000	_____
15.000 000 000	_____	35.000 000 000	_____
16.000 000 000	_____	36.000 000 000	_____
17.000 000 000	_____	37.000 000 000	_____
18.000 000 000	_____	38.000 000 000	_____
19.000 000 000	_____	39.000 000 000	_____
20.000 000 000	_____	40.000 000 000	_____

* Specification for all frequencies listed above is ±100 Hz.

3-6. Frequency Synthesis Tests

Fine Loop Test Procedure (Standard 68169A)

Test Frequency (in Ghz)	Measured Value **
1.000 001 000	_____
1.000 002 000	_____
1.000 003 000	_____
1.000 004 000	_____
1.000 005 000	_____
1.000 006 000	_____
1.000 007 000	_____
1.000 008 000	_____
1.000 009 000	_____
1.000 010 000	_____

** Specifications for all frequencies listed above is ±100 Hz.

Fine Loop Test Procedure (68169A with Option 11)

Test Frequency (in Ghz)	Measured Value ***
1.000 000 100	_____
1.000 000 200	_____
1.000 000 300	_____
1.000 000 400	_____
1.000 000 500	_____
1.000 000 600	_____
1.000 000 700	_____
1.000 000 800	_____
1.000 000 900	_____
1.000 001 000	_____

*** Specification for all frequencies listed above is ±10 Hz.

3-7. Spurious Signals Test: RF Output Signals <2 GHz

Test Procedure	Measured Value	Upper Limit
Set F1 to 10 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 20 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 30 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 40 MHz Record the presence of the worst case harmonic	_____dBc	–30 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 350 MHz Record the presence of the worst case harmonic	_____dBc	–40 dBc
Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the presence of the worst case non-harmonic	_____dBc	–40 dBc
Set F1 to 1.6 GHz Record the level of the harmonics of the 1.6 GHz carrier: 3.2 GHz (2nd harmonic)	_____dBc	–40 dBc
4.8 GHz (3rd harmonic)	_____dBc	–40 dBc

3-8. Harmonic Test: RF Output Signals From 2 to 20 GHz

Test Procedure (2 to 10 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 2.1 GHz Record the level of all harmonics of the 2.1 GHz carrier:		
4.2 GHz (2nd harmonic)	_____dBc	–60 dBc
6.3 GHz (3rd harmonic)	_____dBc	–60 dBc
8.4 GHz (4th harmonic)	_____dBc	–60 dBc
10.5 GHz (5th harmonic)	_____dBc	–60 dBc
12.6 GHz (6th harmonic)	_____dBc	–60 dBc
14.7 GHz (7th harmonic)	_____dBc	–60 dBc
16.8 GHz (8th harmonic)	_____dBc	–60 dBc
18.9 GHz (9th harmonic)	_____dBc	–60 dBc
Set F1 to 3.6 GHz Record the level of all harmonics of the 3.6 GHz carrier:		
7.2 GHz (2nd harmonic)	_____dBc	–60 dBc
10.8 GHz (3rd harmonic)	_____dBc	–60 dBc
14.4 GHz (4th harmonic)	_____dBc	–60 dBc
18.0 Ghz (5th harmonic)	_____dBc	–60 dBc
Set F1 to 7.0 GHz Record the level of all harmonics of the 7 GHz carrier:		
14.0 GHz (2nd harmonic)	_____dBc	–60 dBc
Set F1 to 10.0 GHz Record the level of all harmonics of the 10 GHz carrier:		
20.0 GHz (2nd harmonic)	_____dBc	–60 dBc

Test Procedure (11 to 20 GHz)	**Measure Value**	**Upper Limit**
Set F1 to 12.4 GHz Record the level of all harmonics of the 12.4 GHz carrier:		
24.8 GHz (2nd harmonic)	_____dBc	–60 dBc
37.2 GHz (3rd harmonic)	_____dBc	–60 dBc
Set F1 to 16.0 GHz Record the level of all harmonics of the 16.0 GHz carrier:		
32.0 GHz (2nd harmonic)	_____dBc	–60 dBc
Set F1 to 20.0 GHz Record the level of all harmonics of the 20.0 GHz carrier:		
40.0 GHz (2nd harmonic)	_____dBc	–60 dBc

3-9. Single Sideband Phase Noise Test

Test Procedure	Measured Value	Upper Limit
Set F1 to 5.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–67 dBc
1 kHz	_____dBc	–75 dBc
10 kHz	_____dBc	–83 dBc
100 kHz	_____dBc	–87 dBc
Set F1 to 15.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–58 dBc
1 kHz	_____dBc	–71 dBc
10 kHz	_____dBc	–73 dBc
100 kHz	_____dBc	–82 dBc
Set F1 to 26.0 GHz Record the phase noise levels at these offsets:		
100 Hz	_____dBc	–52 dBc
1 kHz	_____dBc	–65 dBc
10 kHz	_____dBc	–67 dBc
100 kHz	_____dBc	–76 dBc

3-10. Power Level Accuracy and Flatness Tests (68169A Models without Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 26.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 6dBm	_____dBm	+ 6dBm	_____dBm	+ 6dBm	_____dBm
+ 5 dBm	_____dBm	+ 5 dBm	_____dBm	+ 5 dBm	_____dBm
+ 4 dBm	_____dBm	+ 4 dBm	_____dBm	+ 4 dBm	_____dBm
+ 3 dBm	_____dBm	+ 3 dBm	_____dBm	+ 3 dBm	_____dBm
+ 2dBm	_____dBm	+ 2dBm	_____dBm	+ 2dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 1 dBm	_____dBm
– 2 dBm	_____dBm	– 2 dBm	_____dBm	– 2 dBm	_____dBm
– 3 dBm	_____dBm	– 3 dBm	_____dBm	– 3 dBm	_____dBm
– 4 dBm	_____dBm	– 4 dBm	_____dBm	– 4 dBm	_____dBm
– 5 dBm	_____dBm	– 5 dBm	_____dBm	– 5 dBm	_____dBm
– 6 dBm	_____dBm	– 6 dBm	_____dBm	– 6 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 6 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+ 6 dBm	_____dBm	_____dBm	_____dB

3-10. Power Level Accuracy and Flatness Tests (68169A Models with Option 2B Step Attenuator)

Power Level Accuracy Test Procedure

Set F1 to 1.0 GHz		Set F1 to 5.0 GHz		Set F1 to 26.0 GHz	
Set L1 to:	**Measured Power ***	**Set L1 to:**	**Measured Power ***	**Set L1 to:**	**Measured Power ***
+ 2 dBm	_____dBm	+ 2 dBm	_____dBm	+ 2 dBm	_____dBm
+ 1 dBm	_____dBm	+ 1 dBm	_____dBm	+ 1 dBm	_____dBm
+ 0 dBm	_____dBm	+ 0 dBm	_____dBm	+ 0 dBm	_____dBm
– 1 dBm	_____dBm	– 1 dBm	_____dBm	– 1 dBm	_____dBm
– 2 dBm	_____dBm	– 2 dBm	_____dBm	– 2 dBm	_____dBm
– 3 dBm	_____dBm	– 3 dBm	_____dBm	– 3 dBm	_____dBm
– 4 dBm	_____dBm	– 4 dBm	_____dBm	– 4 dBm	_____dBm
– 5 dBm	_____dBm	– 5 dBm	_____dBm	– 5 dBm	_____dBm
– 6 dBm	_____dBm	– 6 dBm	_____dBm	– 6 dBm	_____dBm
– 7 dBm	_____dBm	– 7 dBm	_____dBm	– 7 dBm	_____dBm
– 8 dBm	_____dBm	– 8 dBm	_____dBm	– 8 dBm	_____dBm
– 9 dBm	_____dBm	– 9 dBm	_____dBm	– 9 dBm	_____dBm
–10 dBm	_____dBm	–10 dBm	_____dBm	–10 dBm	_____dBm

* Power Level Accuracy Specification is ±1.0 dB.

Power Level Flatness Test Procedure (Step Sweep)

Set L1 to:	Max Power	Min Power	Variation **
+ 2 dBm	_____dBm	_____dBm	_____dB

** Maximum variation is 1.6 dB.

Power Level Flatness Test Procedure (Analog Sweep)

Set L1 to:	Max Power	Min Power	Variation ***
+ 2 dBm	_____dBm	_____dBm	_____dB

*** Maximum variation is 2.0 dB (0.01 to 20 GHz); 4.0 dB (20 to 40 GHz)(typical, not a specification).

WILTRON Model 68169A **Date:** _____

Serial Number _____ **Calibrated By:** _____

4-7. Preliminary Calibration

Procedure Step	**Step Completion**
Reset the Linearizer DACs	_____
1. Internal DVM Calibration (calterm119)	_____
2. Coarse Loop Pretune DAC Calibration (calterm 137)	_____
3. Fine Loop Pretune DAC Calibration (calterm 136)	_____
4. Sweep Time DAC Calibration (calterm 132)	_____
5. Center Frequency DAC Calibration (calterm 114)	_____
6. YIG Frequency Offset DAC Calibration (calterm 134)	_____
7. YIG Frequency Linearizer DACs Calibration (calterm 127)	_____
8. 100 MHz Reference Oscillator Calibration (calterm 130)	_____
9. FM Coil Sensitivity Calibration DAC Calibration (calterm 135)	_____
10. Sweep Width DAC Calibration (calterm 133)	_____
11. FEU Input Power Levels Calibration (calterm 140) (*This step only applies to units that contain a FEU; i.e., Models 68169A that have serial numbers below 320001*)	_____
12. Store the Calibration Data	_____

4-8. Switched Filter Shaper Calibration

Minimum Unleveled Power Point Measurement **Measured Frequency**

5. Record the minimum unleveled power point frequency for each frequency band:
   - Band 0 (0.01-2.0 GHz) . . . . . _____GHz
   - Band 1 (2.0-3.3 GHz) . . . . . _____GHz
   - Band 2 (3.3-5.5 GHz) . . . . . _____GHz
   - Band 3 (5.5-8.4 GHz) . . . . . _____GHz
   - Band 4 (8.4-13.25 GHz) . . . . . _____GHz
   - Band 5 (13.25-20.0 GHz) . . . . . _____GHz

   The following applies only to units containing a FEU:
   - Band 6 (20.0-26.5 GHz) . . . . . _____GHz
   - Band 7 (26.5-33.0 GHz) . . . . . _____GHz
   - Band 8 (33.0-40.0 GHz) . . . . . _____GHz

Shaper DAC Adjustment **DAC Setting Value**

4.c Record the DAC's setting value for each frequency band:
   - Band 0 (0.01-2.0 GHz) . . . . . _____
   - Band 1 (2.0-3.3 GHz) . . . . . _____
   - Band 2 (3.3-5.5 GHz) . . . . . _____
   - Band 3 (5.5-8.4 GHz) . . . . . _____
   - Band 4 (8.4-13.25 GHz) . . . . . _____
   - Band 5 (13.25-20.0 GHz) . . . . . _____

   The following applies only to units containing a FEU:
   - Band 6 (20.0-26.5 GHz) . . . . . _____
   - Band 7 (26.5-33.0 GHz) . . . . . _____
   - Band 8 (33.0-40.0 GHz) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):
   - Select Item 3 for Band 0 (0.01-2.0 GHz) . . . . . _____
   - Select Item 4 for Band 1 (2.0-3.3 GHz) . . . . . _____
   - Select Item 5 for Band 2 (3.3-5.5 GHz) . . . . . _____
   - Select Item 6 for Band 3 (5.5-8.4 GHz) . . . . . _____
   - Select Item 7 for Band 4 (8.4-13.25 GHz) . . . . . _____

4-8. Switched Filter Shaper Calibration (Continued)

Enter DAC Settings (Continued) **Step Completion**

1.b Select Item 8 for Band 5 (13.25-20.0 GHz) . . . . . _____

The following applies only to units containing a FEU:

Select Item 9 for Band 6 (20.0-26.5 GHz) . . . . . _____

Select Item 10 for Band 7 (26.5-33.0 GHz) . . . . . _____

Select Item 11 for Band 8 (33.0-40.0 GHz) . . . . . _____

Store DAC Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-9. ALC Slope Calibration

Procedure Step **Step Completion**

5. ALC Slope DAC adjustment for ≤2 GHz . . . . . _____

9. ALC Slope DAC adjustment for >2 GHz . . . . . _____

10. Store the DAC setting value(s) . . . . . _____

4-10. RF Level Calibration

This calibration is performed using an automatic test system. Contact AWSC Customer Service for further information.

4-11. AM Bandwidth Calibration

AM Bandwidth Adjustment **DAC Setting Value**

5.c Record the DAC's setting value for each frequency band:

Band 0 (0.01-2.0 GHz) . . . . . _____

Band 1 (2.0-3.3 GHz) . . . . . _____

Band 2 (3.3-5.5 GHz) . . . . . _____

Band 3 (5.5-8.4 GHz) . . . . . _____

Band 4 (8.4-13.25 GHz) . . . . . _____

Band 5 (13.25-20.0 GHz) . . . . . _____

Band 6 (20.0-26.5 GHz w/FEU)/(20.0-25.0 GHz w/SDM) . . . . . _____

Band 7 (26.5-33.0 GHz w/FEU)/(25.0-32.0 GHz w/SDM) . . . . . _____

Band 8 (33.0-40.0 GHz w/FEU)/(32.0-40.0 GHz w/SDM) . . . . . _____

Enter DAC Settings **Step Completion**

1.b Select the menu item for the DAC setting to be updated, then enter the new DAC setting value (recorded above):

Select Item 21 for Band 0 (0.01-2.0 GHz) . . . . . _____

Select Item 22 for Band 1 (2.0-3.3 GHz) . . . . . _____

Select Item 23 for Band 2 (3.3-5.5 GHz) . . . . . _____

Select Item 24 for Band 3 (5.5-8.4 GHz) . . . . . _____

Select Item 25 for Band 4 (8.4-13.25 GHz) . . . . . _____

Select Item 26 for Band 5 (13.25-20.0 GHz) . . . . . _____

Select Item 27 for Band 6 (20.0-26.5 GHz w/FEU)/(20.0-25.0 GHz w/SDM) . . . . . _____

Select Item 28 for Band 7 (26.5-33.0 GHz w/FEU)/(25.0-32.0 GHz w/SDM) . . . . . _____

Select Item 29 for Band 8 (33.0-40.0 GHz w/FEU)/(32.0-40.0 GHz w/SDM) . . . . . _____

Store Dac Settings **Step Completion**

1. Store the DAC setting values . . . . . _____

4-12. AM Calibration

Procedure Step	Step Completion
2. Linear AM Calibration (calterm 112)	_____
3. Log AM Calibration (calterm 113)	_____
4. Store the Calibration Data	_____

4-13. FM Calibration

Procedure Step	Step Completion
2. FM Meter Calibration (calterm 123)	_____
3. FM Wide Sensitivity Calibration (calterm 124)	_____
4. FM Narrow Sensitivity Calibration (calterm 125)	_____
5. Store the Calibration Data	_____